

MODEL NAME : VAW01  
PROJECT CODE : ANRVAW0100  
PCB NO : LA-9101P (Mars Pro)

DA60000UT00 LA-9101P M/B  
DA40001FO00 LS-9101P POWER BUTTON/B  
DA40001FP00 LS-9102P USB/B  
DA40001FQ00 LS-9103P TP BUTTON/B



ZZZ R1@  
PCB VAW01 LA-9101P LS-9101P/9102P/9103P  
DAZ0U500100



ZZZ GCER3@  
PCB VAW01 LA-9101P LS-9101P/9102P/9103P GOLD A31 !  
DAZ0U500101



ZZZ TRIR3@  
PCB VAW00 LA-9101P LS-9101P/9102P/9103P TRIPOD A31 !  
DAZ0U500102



ZZZ HANNR3@  
PCB VAW00 LA-9101P LS-9101P/9102P/9103P HANNSTARB A31 !  
DAZ0U500103



ZZZ ZDTR3@  
PCB VAW00 LA-9101P LS-9101P/9102P/9103P ZDT A31 !  
DAZ0U500104

# Dell / Compal Confidential

## Schematic Document

### Intel Chief River

### Ivy Bridge (BGA) + Panther Point

### OAK 15" UMA/DIS AMD Mars Pro

2012-08-22

Rev: 0.4

46@ : for 46 level

@ : Nopop Component

CONN@ : Connector Component

KB9012@ : ENE KB9012 Implemented

UMA@ : Only for UMA

EMC@ : EMI/ESD parts

GCLK@ : Green CLK implemented

GCLKUMA@ : Green CLK for UMA

GCLKDIS@ : Green CLK for DIS

XTAL@ : X'tal implemented

XTALDIS@ : X'tal with DIS implemented

R1@ : R1 P/N

R3@ : R3 P/N

i3R1@ : CPU i3-3217 1.8G

i3VOSR1@ : CPU i3-2365 1.4G

i5R1@ : CPU i5-3317 1.7G

i7R1@ : CPU i7-3517 1.9G

CEL1@ : CPU Celeron 887 1.5G

PENR1@ : CPU Pentium 997 1.6G

DIS@ : Only for Discrete

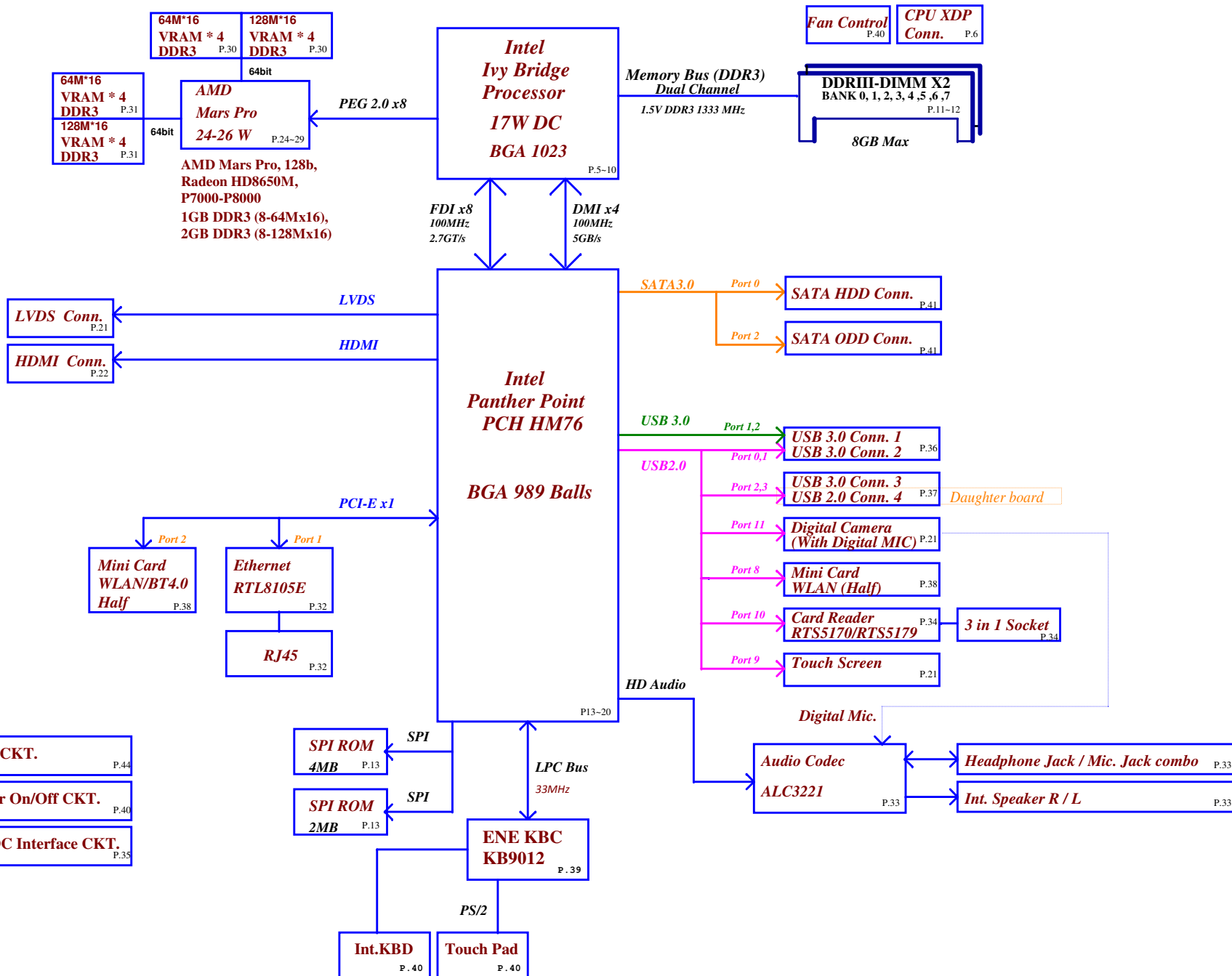
TH@/THR1@ : Thames-XT

MS@/MSR1@ : Mars Pro

X76@ :

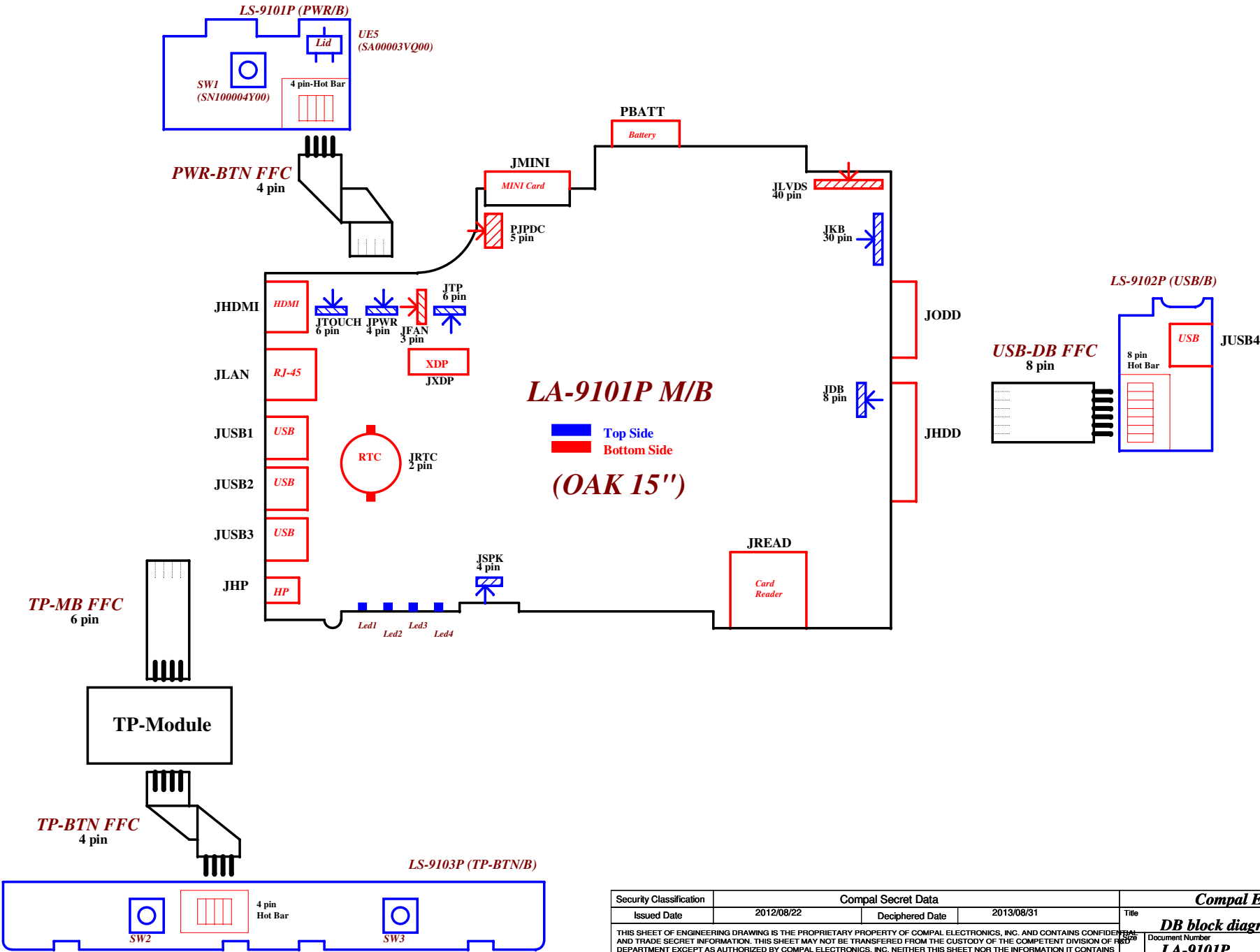
SPI-ROM & VRAM Group

|   |                    |                 |            |                          |                            |
|---|--------------------|-----------------|------------|--------------------------|----------------------------|
| Security Classification   | Compal Secret Data |                 |            | Compal Electronics, Inc. |                            |
| Issued Date   | 2012/08/22         | Deciphered Date | 2013/08/31 | Title                    | Cover Page                 |
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|   |                    |                 |            | Date                     | Wednesday, August 28, 2012 |
|   |                    |                 |            | Sheet                    | 1 of 57                    |
|   |                    |                 |            | Rev                      | 0.4                        |



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Project Code : VAW01  
File Name : LA-9101P



|   |            |                    |            |                          |                            |
|---|------------|--------------------|------------|--------------------------|----------------------------|
| Security Classification   |            | Compal Secret Data |            | Compal Electronics, Inc. |                            |
| Issued Date   | 2012/08/22 | Deciphered Date    | 2013/08/31 | Title                    | DB block diagram           |
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|   |            |                    |            | Date                     | Wednesday, August 29, 2012 |
|   |            |                    |            | Sheet                    | 3 of 57                    |
|   |            |                    |            | Rev                      | 0.4                        |

Board ID Table for AD channel

|          |             |             |             |             |           |
|----------|-------------|-------------|-------------|-------------|-----------|
| Vcc      | 3.3V +/- 5% |             |             |             |           |
| Ra       | 100K +/- 5% |             |             |             |           |
| Board ID | Rb          | VAD_BID min | VAD_BID typ | VAD_BID max | EC AD3    |
| 0        | 0           | 0 V         | 0 V         | 0.155 V     | 0x00-0x0C |
| 1        | 8.2K +/- 5% | 0.168 V     | 0.250 V     | 0.362 V     | 0x0D-0x1C |
| 2        | 18K +/- 5%  | 0.375 V     | 0.503 V     | 0.621 V     | 0x1D-0x30 |
| 3        | 33K +/- 5%  | 0.634 V     | 0.819 V     | 0.945 V     | 0x31-0x49 |
| 4        | 56K +/- 5%  | 0.958 V     | 1.185 V     | 1.359 V     | 0x4A-0x69 |
| 5        | 100K +/- 5% | 1.372 V     | 1.650 V     | 1.838 V     | 0x6A-0x8E |
| 6        | 200K +/- 5% | 1.851 V     | 2.200 V     | 2.420 V     | 0x8F-0xBB |
| 7        | NC          | 2.433 V     | 3.300 V     | 3.300 V     | 0xBC-0xFF |

BOARD ID Table

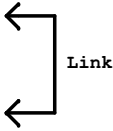
|      |              |
|------|--------------|
| ID   | PCB Revision |
| 0    | 0.1          |
| 1    | 0.1          |
| 2    | 0.2          |
| 3    | 0.2          |
| 4    | 0.3          |
| 5    | 0.4          |
| 6    | 1.0          |
| 7    | 1.0          |
| UMA  | THM          |
| MARS |              |

Project ID Table

|    |                  |
|----|------------------|
| ID | Project Revision |
| 0  |                  |
| 1  |                  |
| 2  |                  |
| 3  |                  |
| 4  |                  |
| 5  | UMA              |
| 6  | DIS THAMES       |
| 7  | DIS MARS PRO     |

SMBUS Control Table

|                             | SOURCE | MINI1 | MINI2 | BATT | SODIMM | Express Card | Thermal Sensor | FFS | VGA Thermal Sensor | VGA | XDP | Charger |
|-----------------------------|--------|-------|-------|------|--------|--------------|----------------|-----|--------------------|-----|-----|---------|
| EC_SMB_CK1<br>EC_SMB_DA1    | KB9012 |       |       | V    |        |              |                |     |                    |     |     | V       |
| EC_SMB_CK2<br>EC_SMB_DA2    | KB9012 |       |       |      |        |              |                |     | V                  | V   |     |         |
| PCH_SML0CLK<br>PCH_SML0DATA | PCH    |       |       |      |        |              |                |     |                    |     |     |         |
| PCH_SML1CLK<br>PCH_SML1DATA | PCH    |       |       |      |        |              |                |     |                    |     |     |         |
| MEM_SMBCLK<br>MEM_SMBDATA   | PCH    | V     | V     |      | V      | V            |                | V   |                    |     | V   |         |



|     |           |                  |
|-----|-----------|------------------|
| PCH | USB PORT# | DESTINATION      |
|     | 0         | USB conn.2       |
|     | 1         | USB conn.1       |
|     | 2         | USB conn.3       |
|     | 3         | USB conn.4 (DB)  |
|     | 4         | NC               |
|     | 5         | NC               |
|     | 6         | NC               |
|     | 7         | NC               |
|     | 8         | MINI CARD (WLAN) |
|     | 9         | Touch Screen     |
|     | 10        | Card Reader      |
|     | 11        | Camera           |
|     | 12        | NC               |
|     | 13        | NC               |

|     |              |                |             |             |
|-----|--------------|----------------|-------------|-------------|
| CLK | DIFFERENTIAL | DESTINATION    | FLEX CLOCKS | DESTINATION |
|     | CLKOUT_PCIE0 | 10/100 LAN     | CLKOUTFLEX0 | None        |
|     | CLKOUT_PCIE1 | MINI CARD WLAN | CLKOUTFLEX1 | None        |
|     | CLKOUT_PCIE2 | None           | CLKOUTFLEX2 | None        |
|     | CLKOUT_PCIE3 | None           | CLKOUTFLEX3 | None        |
|     | CLKOUT_PCIE4 | None           |             |             |
|     | CLKOUT_PCIE5 | None           |             |             |
|     | CLKOUT_PCIE6 | None           |             |             |
|     | CLKOUT_PCIE7 | None           |             |             |
|     | CLKOUT_PEG_B | None           |             |             |

|        |              |
|--------|--------------|
| CLKOUT | DESTINATION  |
| PCI0   | PCH_LOOPBACK |
| PCI1   | EC LPC       |
| PCI2   | None         |
| PCI3   | None         |
| PCI4   | None         |

|       |             |
|-------|-------------|
| SATA  | DESTINATION |
| SATA0 | HDD         |
| SATA1 | None        |
| SATA2 | ODD         |
| SATA3 | None        |
| SATA4 | None        |
| SATA5 | None        |

|             |                  |
|-------------|------------------|
| PCI EXPRESS | DESTINATION      |
| Lane 1      | 10/100 LAN       |
| Lane 2      | MINI CARD (WLAN) |
| Lane 3      | None             |
| Lane 4      | None             |
| Lane 5      | None             |
| Lane 6      | None             |
| Lane 7      | None             |
| Lane 8      | None             |

Symbol Note :



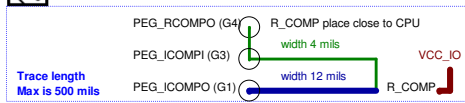
: means Digital Ground



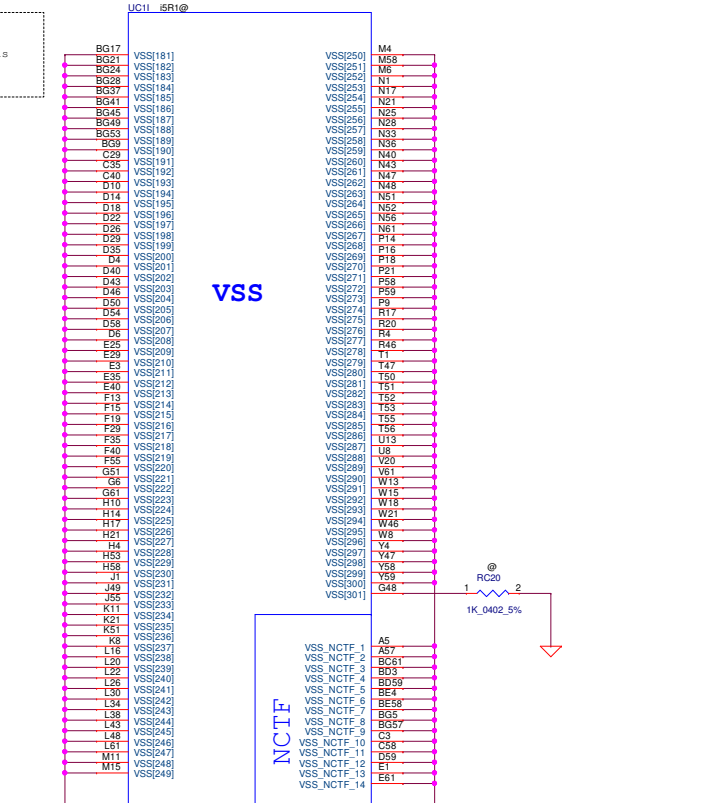
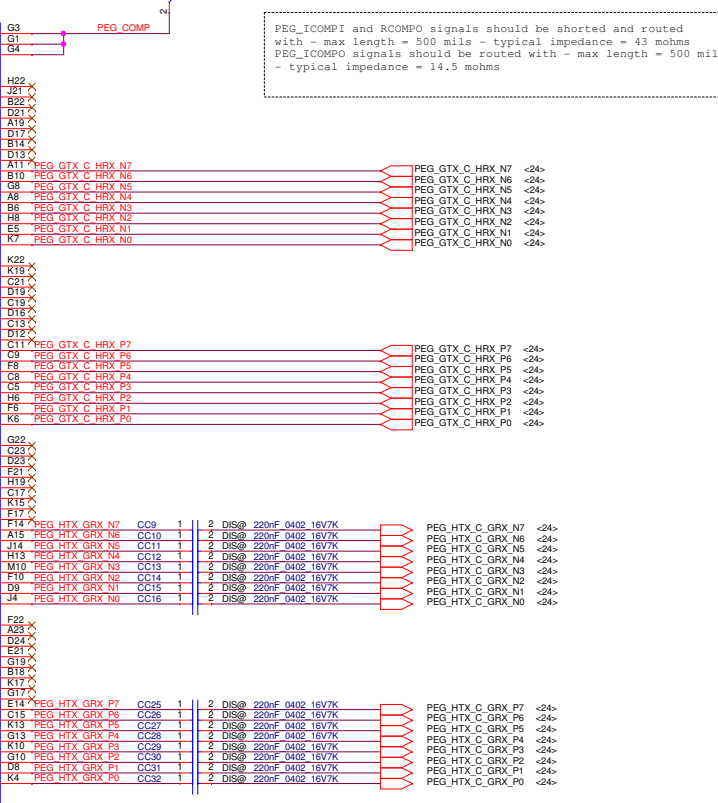
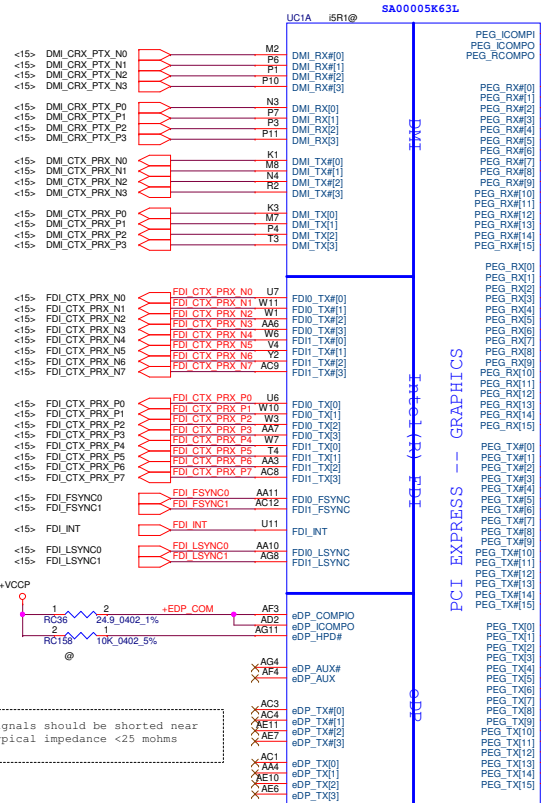
: means Analog Ground

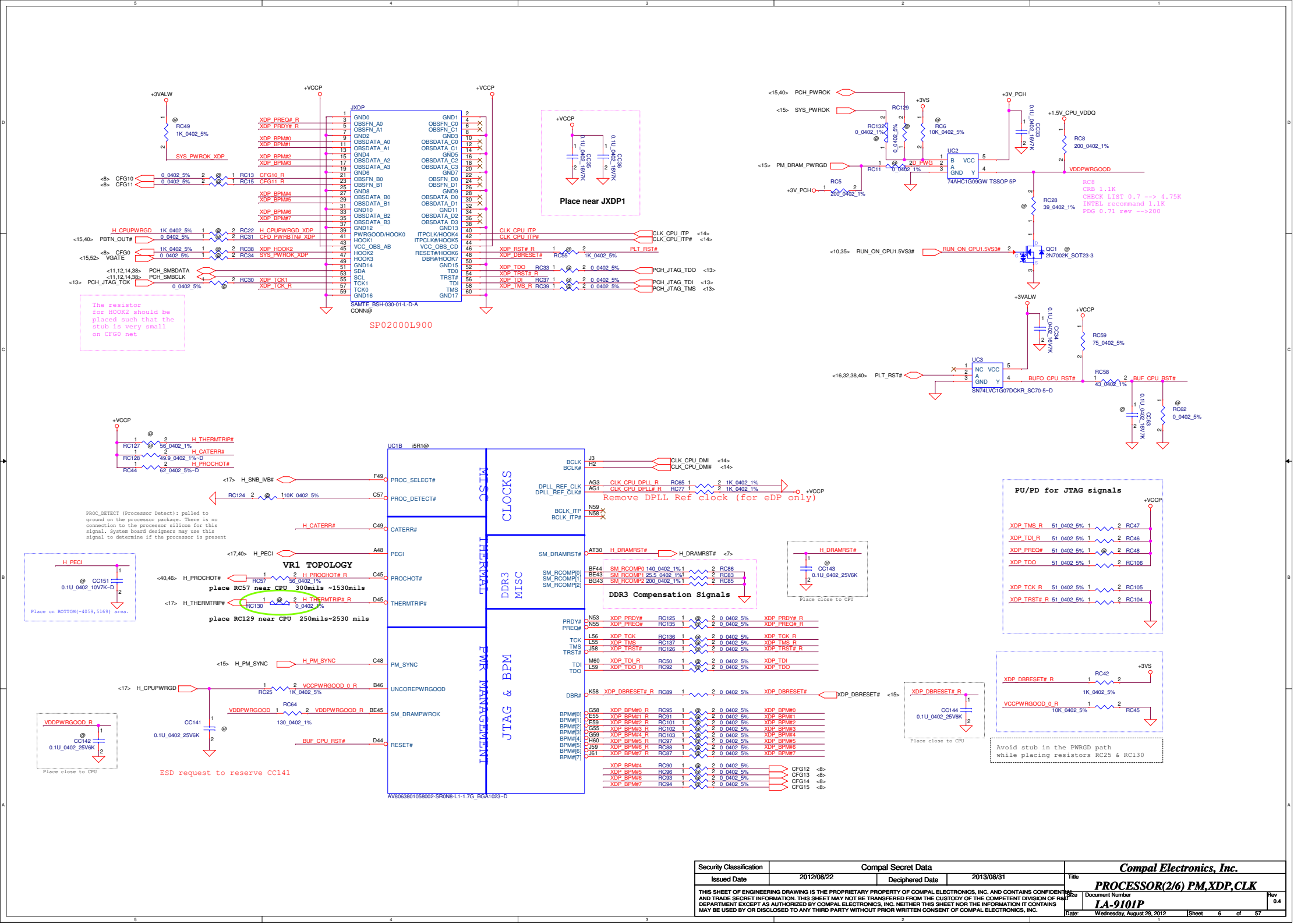


(1) PEG\_RCOMP0 (G4) use 4mil connect to PEG\_ICOMPI, then use 4mil connect to RC1.  
(2) PEG\_ICOMPU use 12mil connect to RC1



PEG\_ICOMPI and RCOMP0 signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms  
PEG\_ICOMPU signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

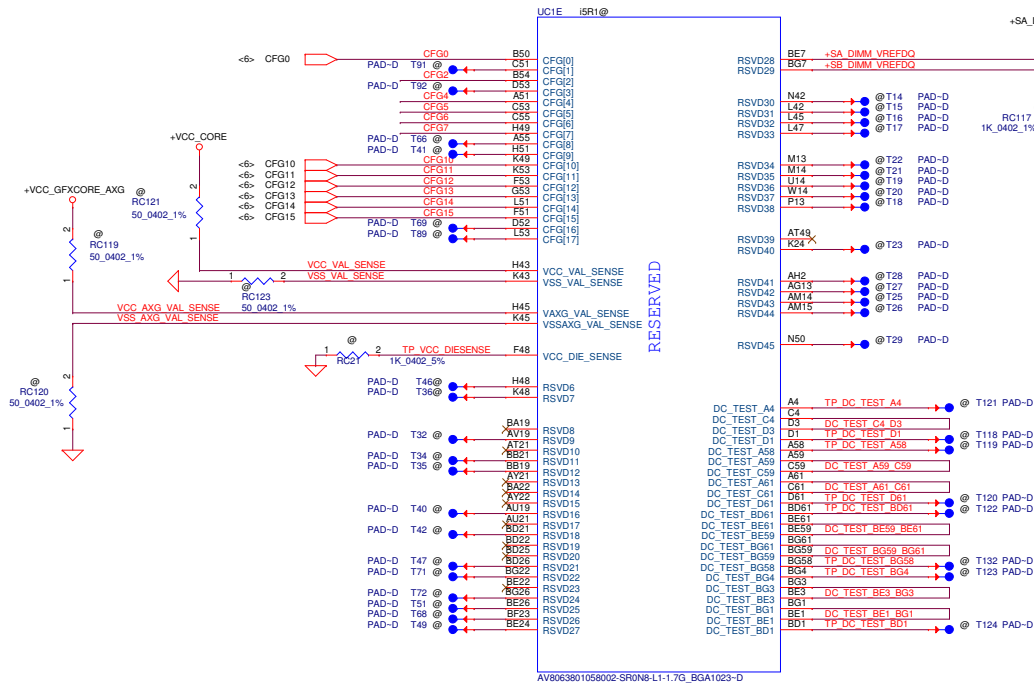








CFG Straps for Processor



| PEG Static Lane Reversal - CFG2 is for the 16x |  |
|--|--|
| CFG2   | 1: (Default) Normal Operation; Lane # definition matches socket pin map definition<br>* 0: Lane Reversed |

| Display Port Presence Strap |  |
|-----------------------------|--|
| CFG4                        | * 1 : Disabled; No Physical Display Port attached to Embedded Display Port<br>0 : Enabled; An external Display Port device is connected to the Embedded Display Port |

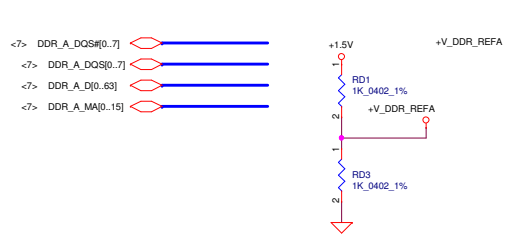
| PCIe Port Bifurcation Straps |  |
|------------------------------|--|
| CFG[6:5]                     | 11: (Default) x16 - Device 1 functions 1 and 2 disabled<br>* 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled<br>01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)<br>00: x8,x4,x4 - Device 1 functions 1 and 2 enabled |

| PEG DEFER TRAINING |   |
|--------------------|---|
| CFG7               | * 1: (Default) PEG Train immediately following xxRESETB de assertion<br>0: PEG Wait for BIOS for training |



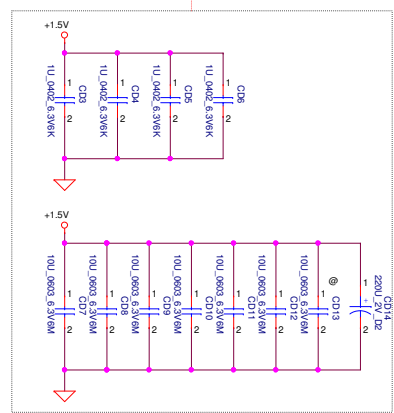




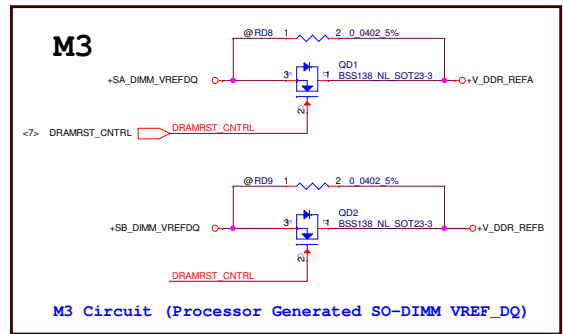
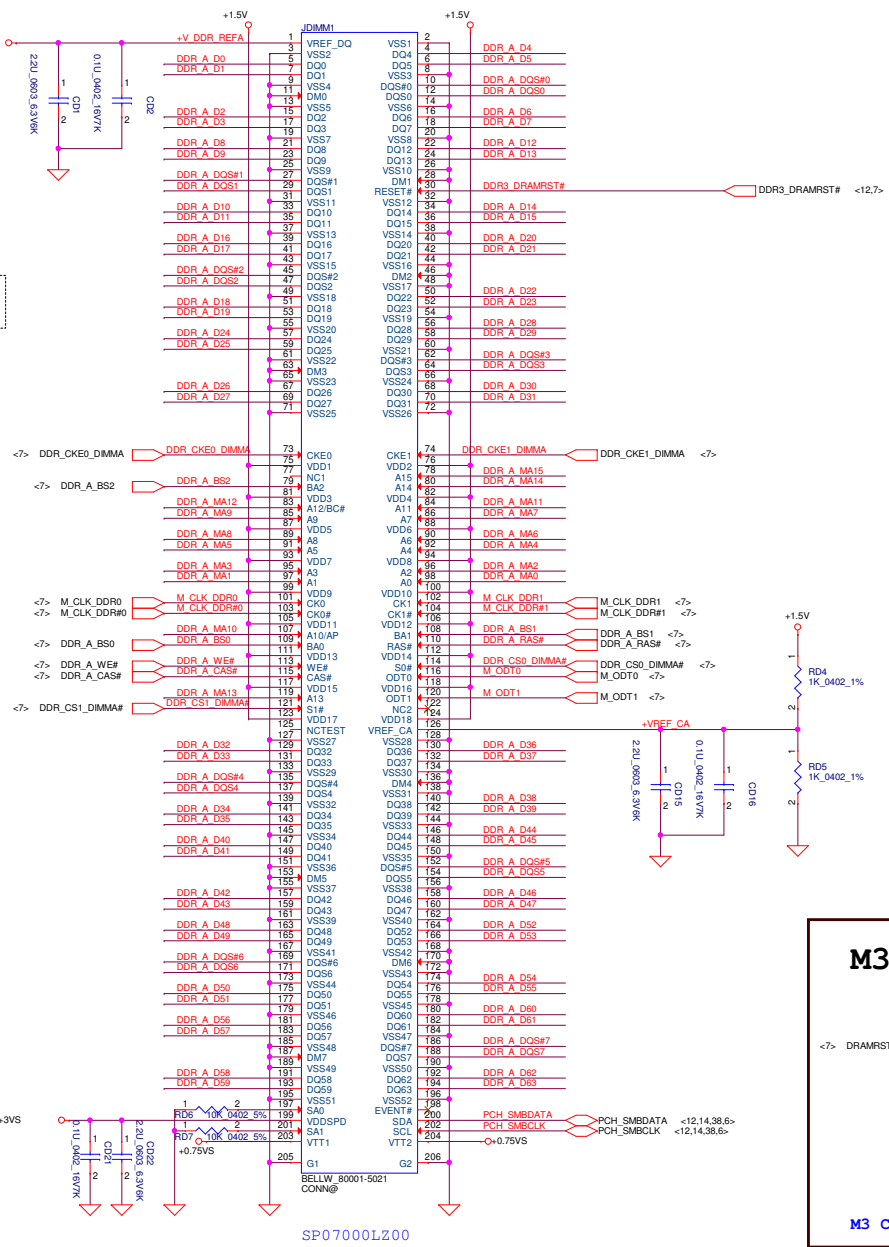
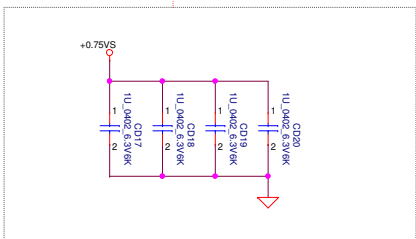


**Layout Note:**  
Place near JDIMM1

All VREF traces should have 10 mil trace width

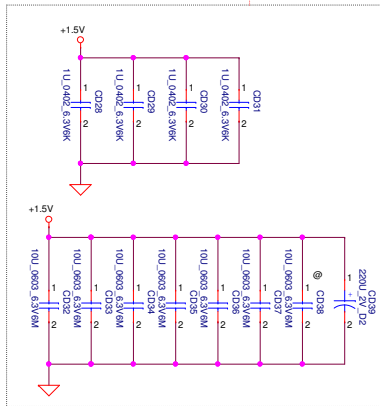


**Layout Note:**  
Place near JDIMM1.203,204

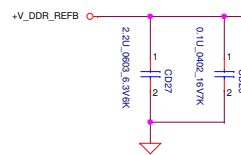
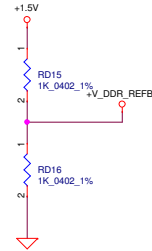
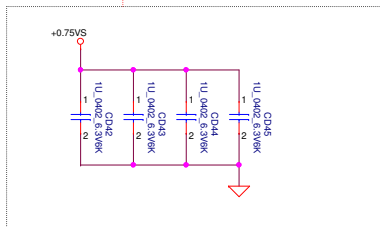




Layout Note:  
Place near JDIMMB

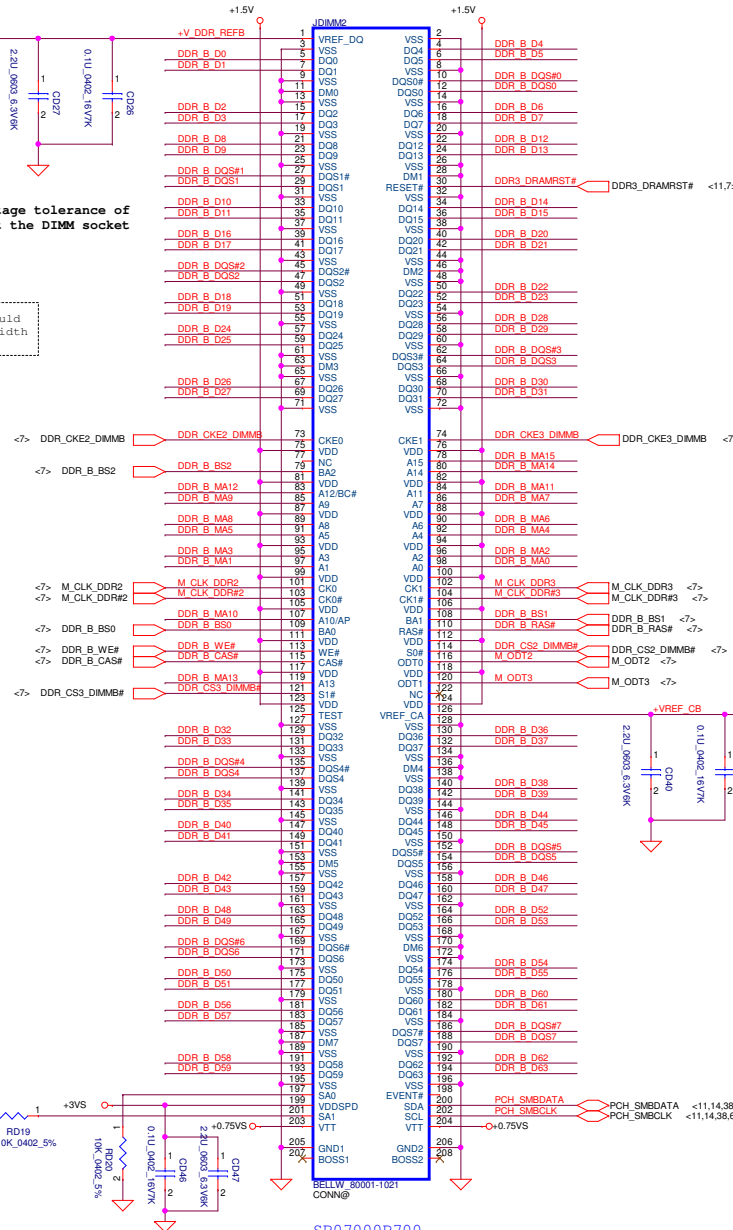


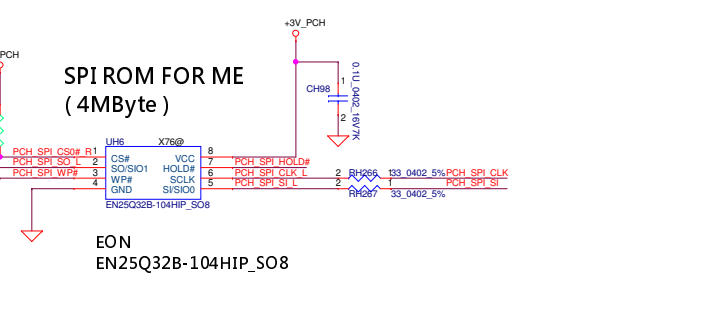
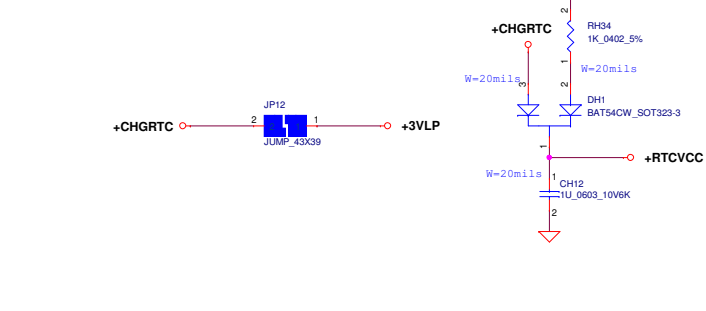
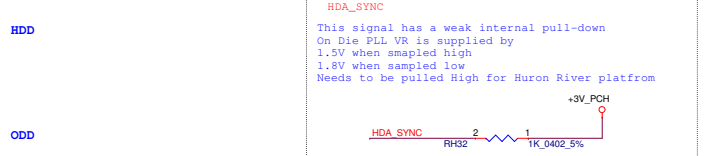
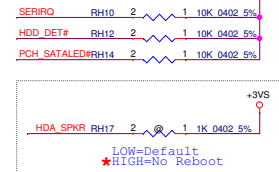
Layout Note:  
Place near JDIMMB.203,204



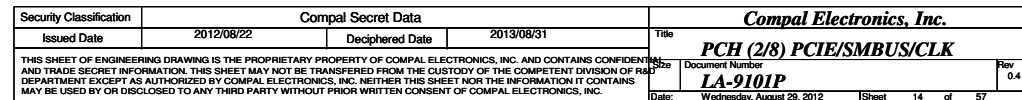
Note:  
Check voltage tolerance of  
VREF\_DQ at the DIMM socket

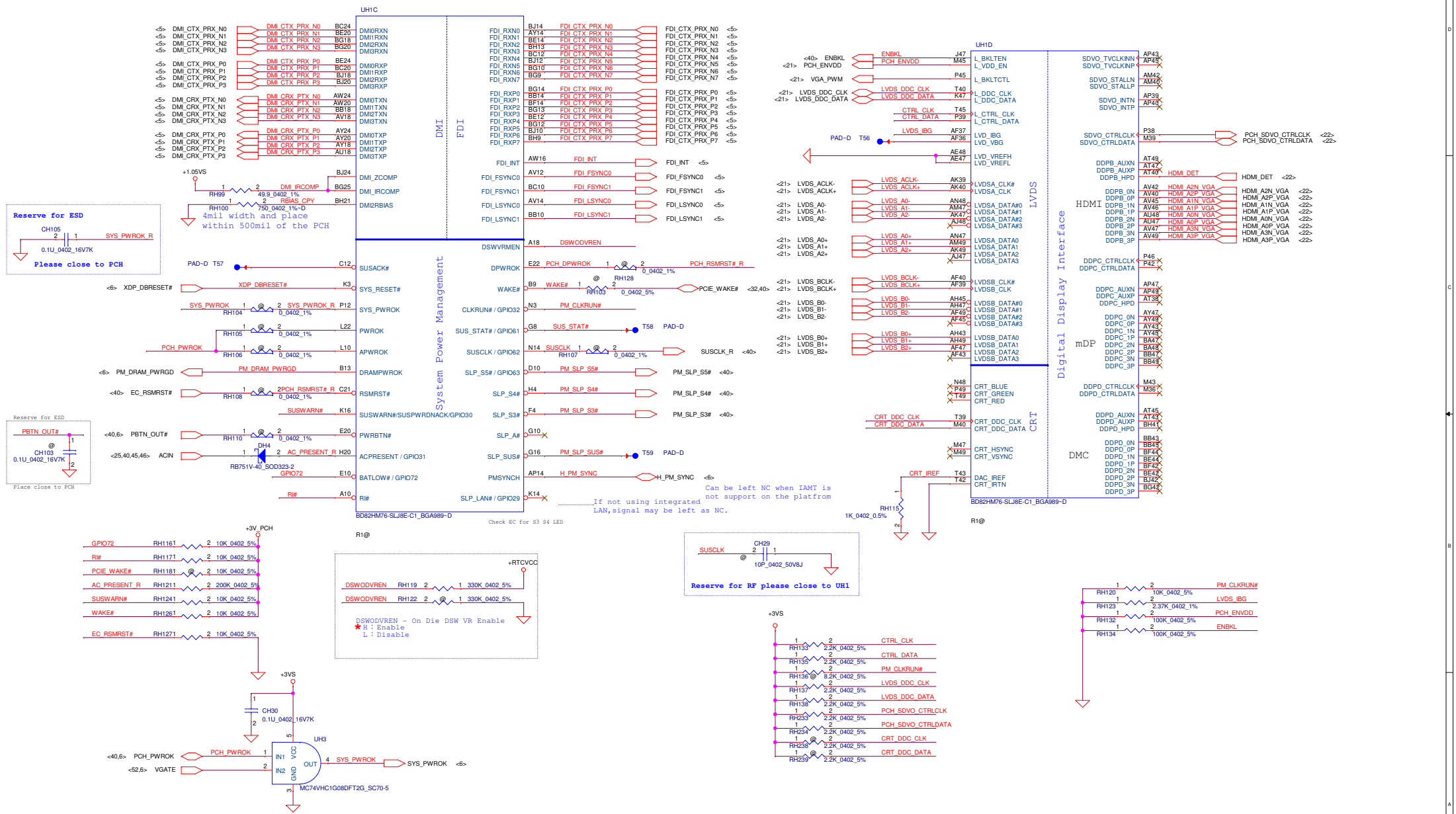
All VREF traces should  
have 10 mil trace width





|  |  |                          |                 |                          |                            |       |
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|  |  |                          |                 |                          | Document Number            | Rev   |
|  |  |                          |                 |                          | LA-9101P                   |       |
| Date:  |  | Wednesday August 26 2012 |                 | Sheet                    | 13                         | of 57 |

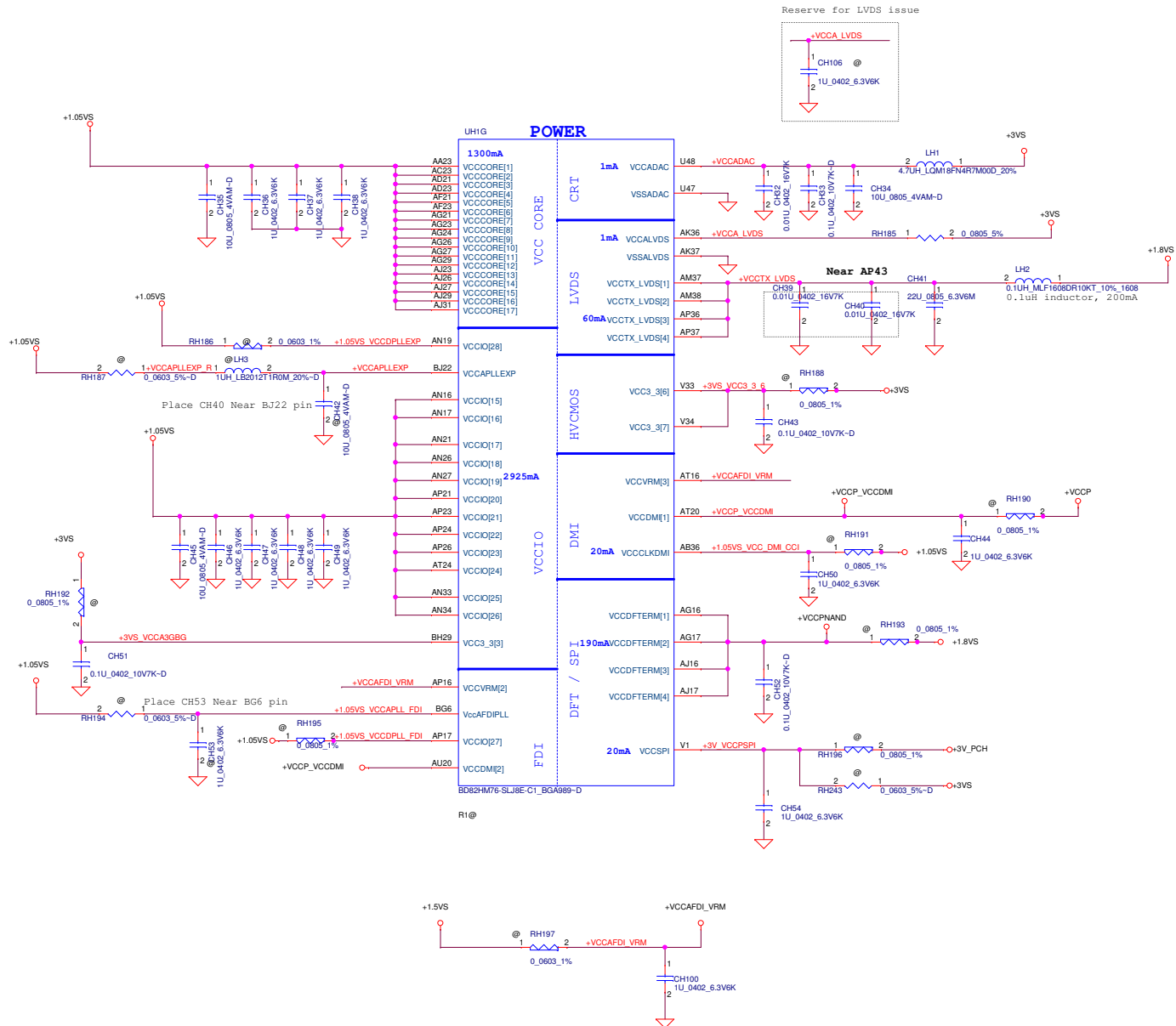




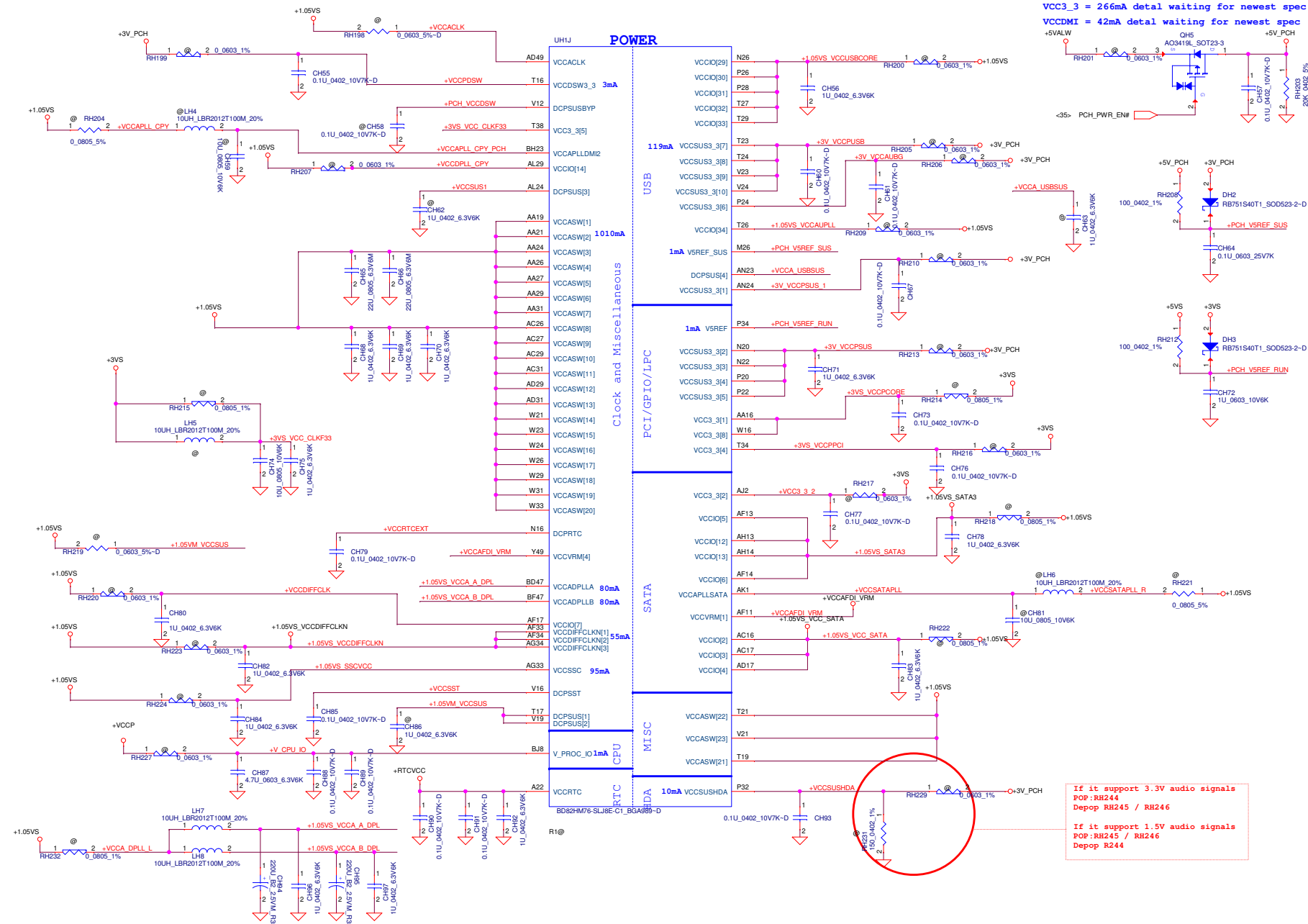








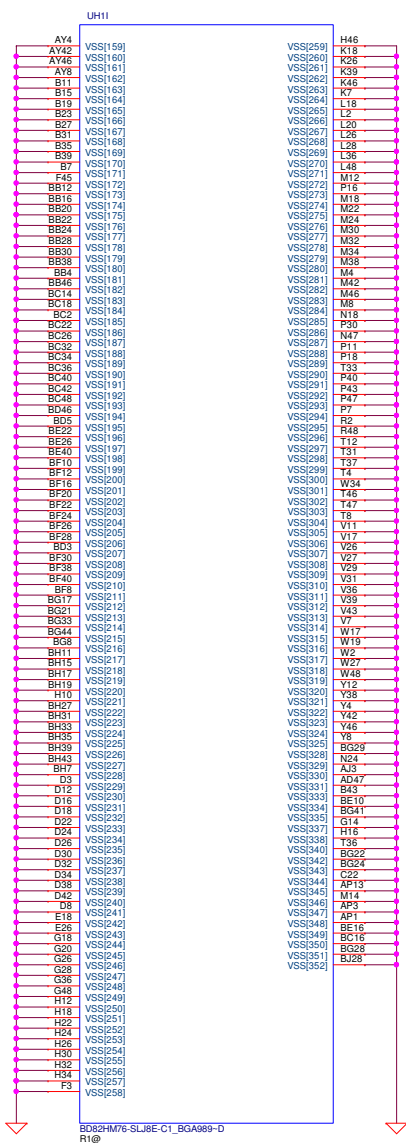
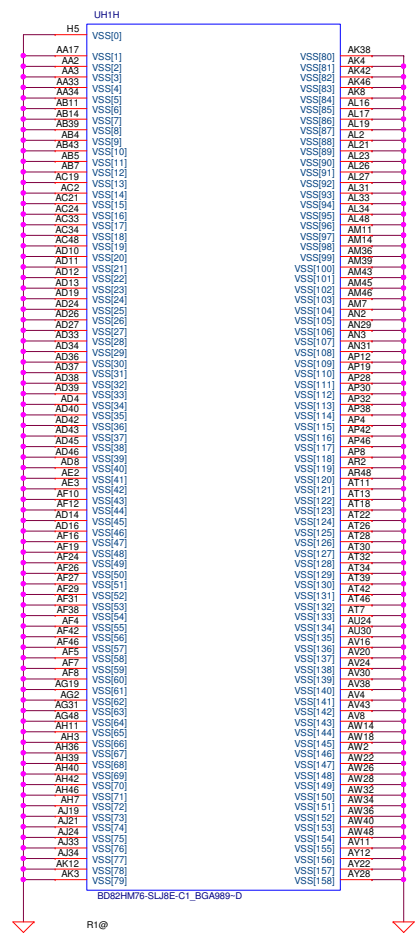
| Voltage Rail | Voltage   | S0 Iccmax Current (A) |
|--------------|-----------|-----------------------|
| V_PROC_IO    | 1.05      | 0.001                 |
| V5REF        | 5         | 0.001                 |
| V5REF_Sus    | 5         | 0.001                 |
| Vcc3_3       | 3.3       | 0.266                 |
| VccADAC      | 3.3       | 0.001                 |
| VccADPLLA    | 1.05      | 0.08                  |
| VccADPLLB    | 1.05      | 0.08                  |
| VccCore      | 1.05      | 1.3                   |
| VccDMI       | 1.05      | 0.042                 |
| VccIO        | 1.05      | 2.925                 |
| VccASW       | 1.05      | 1.01                  |
| VccSPI       | 3.3       | 0.02                  |
| VccDSW       | 3.3       | 0.003                 |
| VccpNAND     | 1.8       | 0.19                  |
| VccRTC       | 3.3       | 6 uA                  |
| VccSus3_3    | 3.3       | 0.119                 |
| VccSusHDA    | 3.3 / 1.5 | 0.01                  |
| VccVRM       | 1.8 / 1.5 | 0.16                  |
| VccCLKDMI    | 1.05      | 0.02                  |
| VccSSC       | 1.05      | 0.095                 |
| VccDIFFCLKN  | 1.05      | 0.055                 |
| VccALVDS     | 3.3       | 0.001                 |
| VccTX_LVDS   | 1.8       | 0.06                  |



VCC3\_3 = 266mA detail waiting for newest spec  
VCCDMI = 42mA detail waiting for newest spec

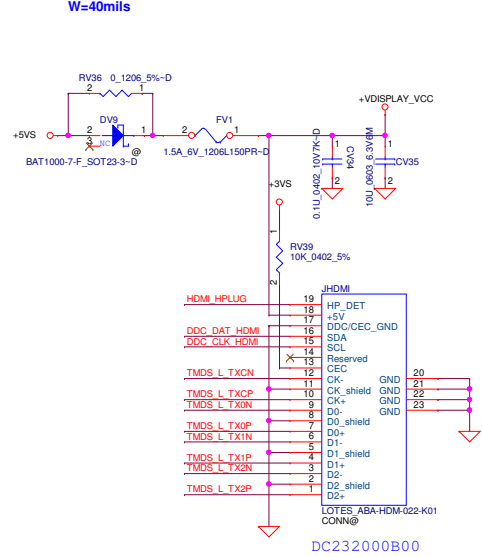
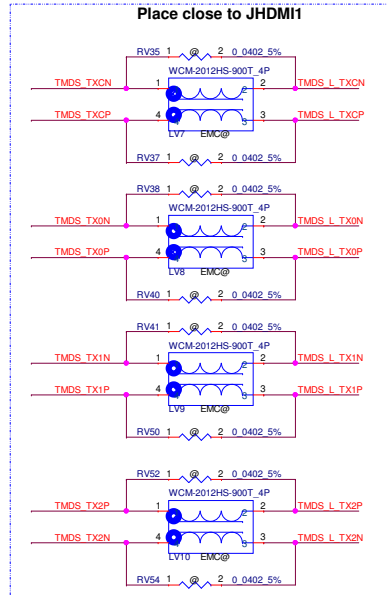
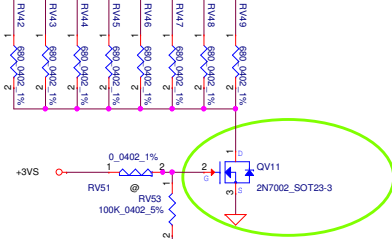
If it support 3.3V audio signals  
POP: RH244 / RH246  
Depop RH244 / RH246

If it support 1.5V audio signals  
POP: RH245 / RH246  
Depop R244





|      |              |      |   |   |      |      |         |           |
|------|--------------|------|---|---|------|------|---------|-----------|
| <15> | HDMI_A3N_VGA | CV32 | 2 | 1 | 0.1U | 0402 | 10V7K-D | TMDS TXCN |
| <15> | HDMI_A3P_VGA | CV33 | 2 | 1 | 0.1U | 0402 | 10V7K-D | TMDS TXCP |
| <15> | HDMI_A0N_VGA | CV36 | 2 | 1 | 0.1U | 0402 | 10V7K-D | TMDS TX0N |
| <15> | HDMI_A0P_VGA | CV37 | 2 | 1 | 0.1U | 0402 | 10V7K-D | TMDS TX0P |
| <15> | HDMI_A1N_VGA | CV38 | 2 | 1 | 0.1U | 0402 | 10V7K-D | TMDS TX1N |
| <15> | HDMI_A1P_VGA | CV39 | 2 | 1 | 0.1U | 0402 | 10V7K-D | TMDS TX1P |
| <15> | HDMI_A2N_VGA | CV40 | 2 | 1 | 0.1U | 0402 | 10V7K-D | TMDS TX2N |
| <15> | HDMI_A2P_VGA | CV41 | 2 | 1 | 0.1U | 0402 | 10V7K-D | TMDS TX2P |

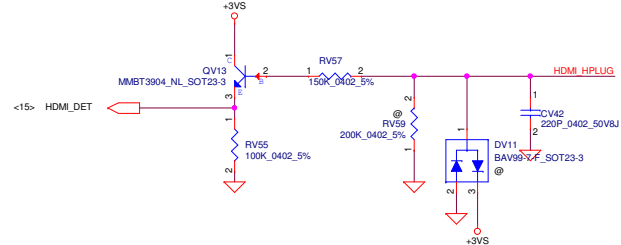
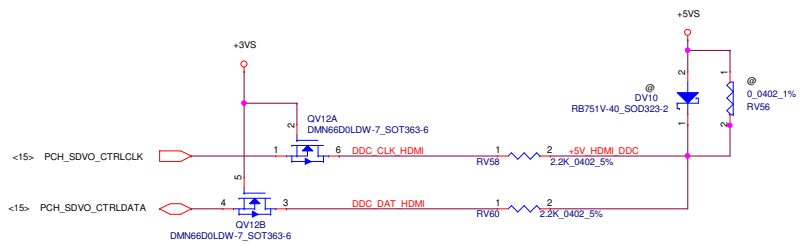


|           |        |   |   |      |      |       |
|-----------|--------|---|---|------|------|-------|
| TMDS TXCN | @CV358 | 1 | 2 | 100P | 0402 | 50V8J |
| TMDS TXCP | @CV360 | 1 | 2 | 100P | 0402 | 50V8J |
| TMDS TX0N | @CV362 | 1 | 2 | 100P | 0402 | 50V8J |
| TMDS TX0P | @CV363 | 1 | 2 | 100P | 0402 | 50V8J |
| TMDS TX1N | @CV359 | 1 | 2 | 100P | 0402 | 50V8J |
| TMDS TX1P | @CV357 | 1 | 2 | 100P | 0402 | 50V8J |
| TMDS TX2N | @CV361 | 1 | 2 | 100P | 0402 | 50V8J |
| TMDS TX2P | @CV364 | 1 | 2 | 100P | 0402 | 50V8J |

20111024 EMI ADD

|             |       |   |   |      |      |         |
|-------------|-------|---|---|------|------|---------|
| TMDS L TXCN | CV349 | 1 | 2 | 3.3P | 0402 | 50V8C-D |
| TMDS L TXCP | CV350 | 1 | 2 | 3.3P | 0402 | 50V8C-D |
| TMDS L TX0N | CV351 | 1 | 2 | 3.3P | 0402 | 50V8C-D |
| TMDS L TX0P | CV352 | 1 | 2 | 3.3P | 0402 | 50V8C-D |
| TMDS L TX1N | CV353 | 1 | 2 | 3.3P | 0402 | 50V8C-D |
| TMDS L TX1P | CV354 | 1 | 2 | 3.3P | 0402 | 50V8C-D |
| TMDS L TX2N | CV355 | 1 | 2 | 3.3P | 0402 | 50V8C-D |
| TMDS L TX2P | CV356 | 1 | 2 | 3.3P | 0402 | 50V8C-D |

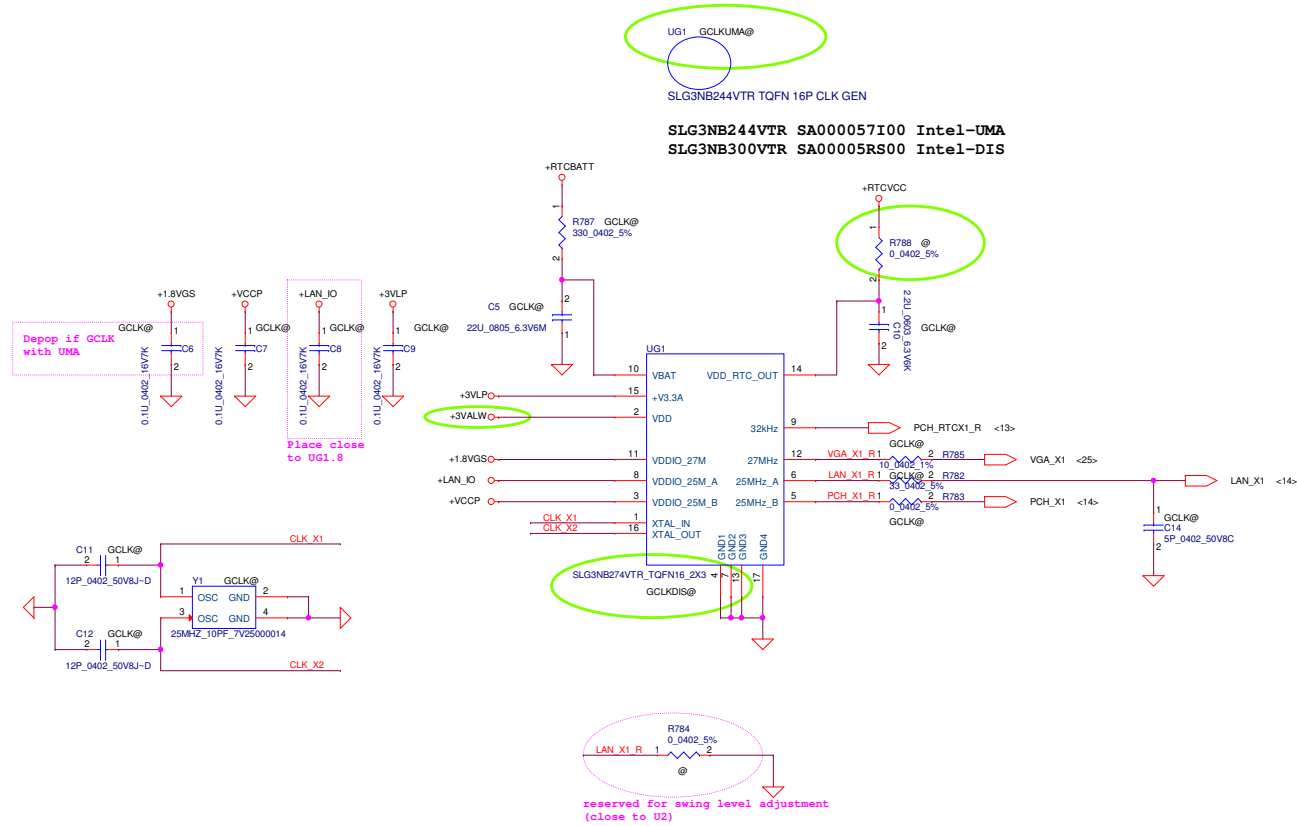
20110805 EMI ADD



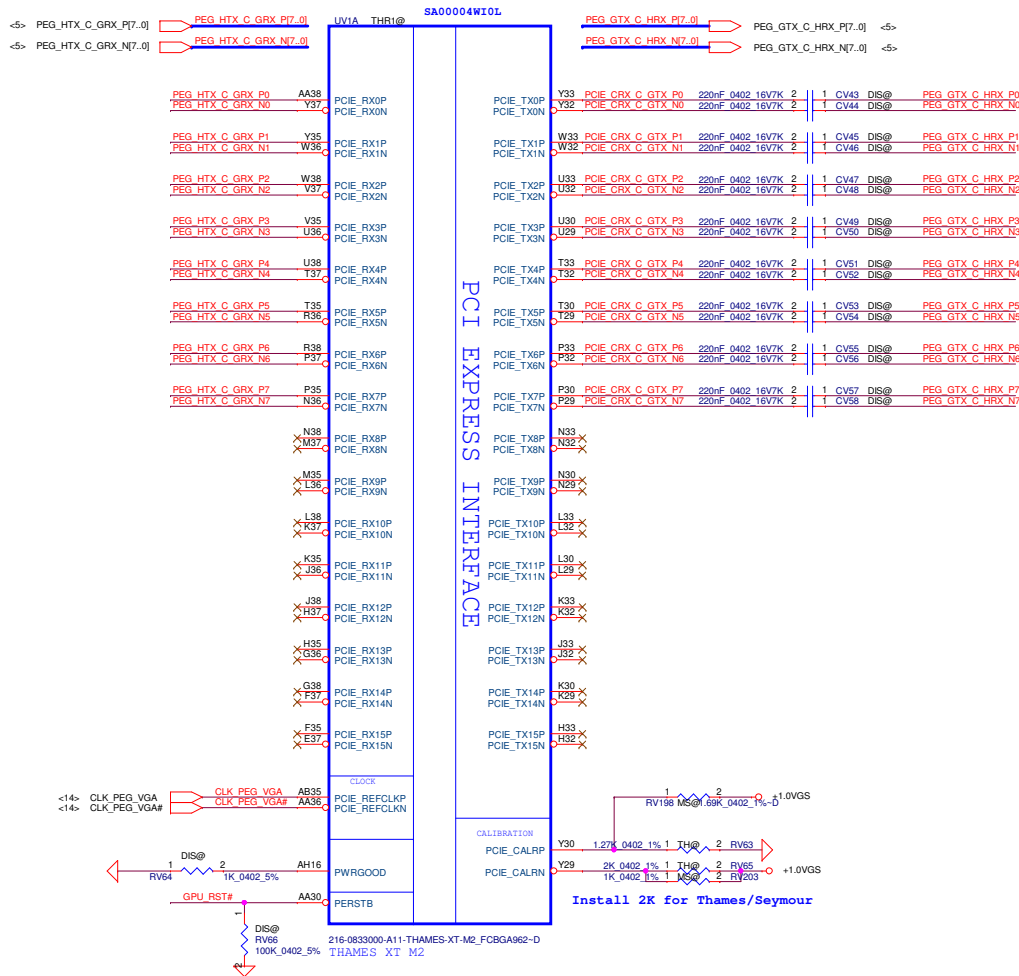
|             |                         |
|-------------|-------------------------|
| 46@         | ROYALTY HDMI W/LOGO     |
| Part Number | Description             |
| 8000000023M | HDMI W/Logo:8000000023M |

|   |                    |                 |                            |
|---|--------------------|-----------------|----------------------------|
| Security Classification   | Compal Secret Data | Title           | 46@                        |
| Issued Date   | 2012/08/22         | Deciphered Date | 2013/08/31                 |
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|   |                    | Date            | Wednesday, August 28, 2012 |
|   |                    | Sheet           | 22 of 57                   |

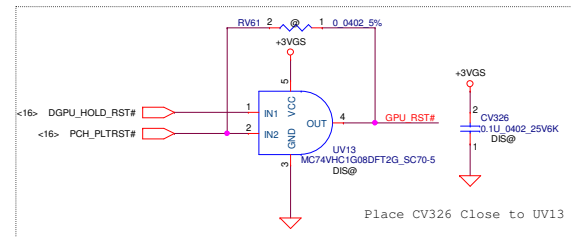
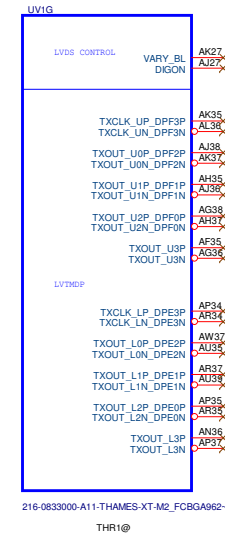




# GFX PCIE LANE REVERSAL



## LVDS Interface



216-0833000-A11-THAMES-XT-M2\_FCBGA962-D



MARS-PRO\_FCBGA962-D

MARS Pro



MARS-PRO\_FCBGA962-D

MARS Pro

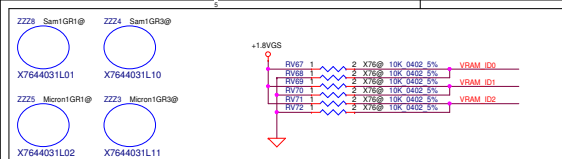


Chelsea Pro



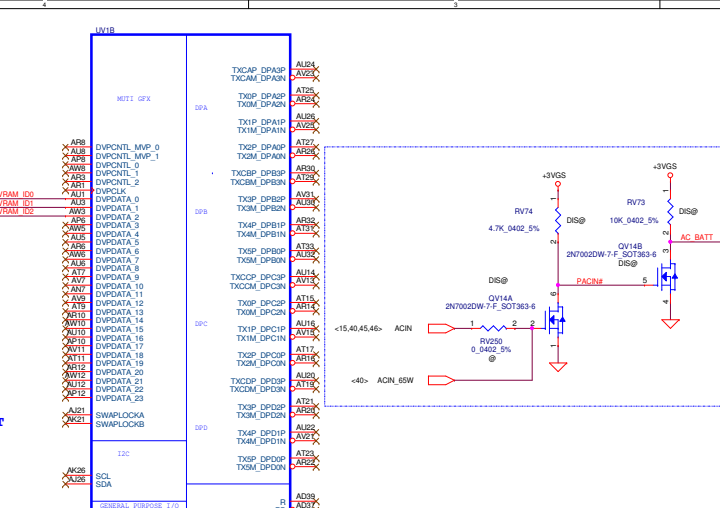
Chelsea Pro

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|---|------------|--------------------|------------|---------------------------|----------------------------|
| Security Classification   |            | Compal Secret Data |            | Title                     |                            |
| Issued Date   | 2012/08/22 | Deciphered Date    | 2013/08/31 | ATI ThamesXT M2 PCIE/LVDS |                            |
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|   |            |                    |            | Date                      | Wednesday, August 28, 2012 |
|   |            |                    |            | Sheet                     | 24 of 57                   |



| Vendor          | VRAM_ID0 | VRAM_ID1 | VRAM_ID2 |
|-----------------|----------|----------|----------|
| Samsung 1GB     |          |          |          |
| SA00004GS0L(R1) | RV68     | RV69     | RV72     |
| SA00004GS1L(R3) | 0        | 1        | 0        |
| Hynix 1GB       |          |          |          |
| SA00004Y20L(R1) | RV67     | RV70     | RV72     |
| SA00004Y21L(R3) | 1        | 0        | 1        |
| Samsung 2GB     |          |          |          |
| SA00005SH0L(R1) | RV68     | RV69     | RV71     |
| SA00005SH1L(R3) | 0        | 1        | 1        |
| Hynix 2GB       |          |          |          |
| SA00003Y02L(R1) | RV67     | RV70     | RV71     |
| SA00003Y03L(R3) | 1        | 0        | 1        |
| Micron 2GB      |          |          |          |
| SA00005XB0L(R1) | RV68     | RV69     | RV71     |
| SA00005XB1L(R3) | 0        | 1        | 1        |

PT



### CONFIGURATION STRAPS

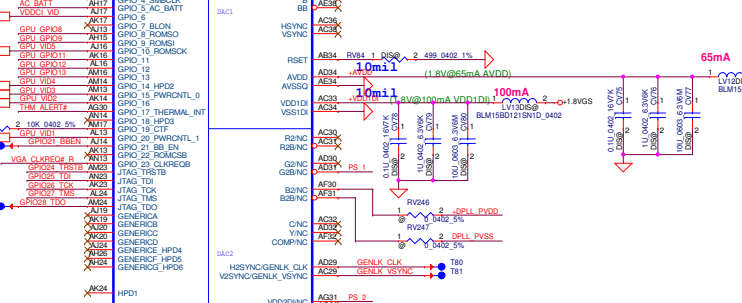
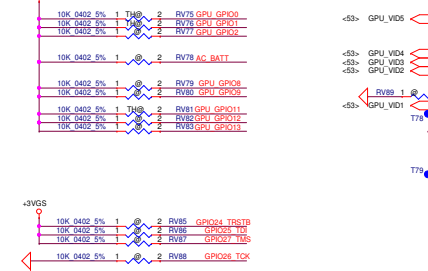
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

| STRAPS              | PN             | DESCRIPTION OF DEFAULT SETTINGS   | RECOMMENDED SETTINGS          | RECOMMENDED SETTINGS |
|---------------------|----------------|---|-------------------------------|----------------------|
| TX_PWRS_ENB         | GPI00          | PCI FULL TX OUTPUT SWING  | 0: 50% swing<br>1: Pull swing | X                    |
| TX_DEEMPH_EN        | GPI01          | PCI TRANSMITTER DE-EMPHASIS   | 0: disable<br>1: enable       | X                    |
| RSVD                | GPI02          | Advertises PCIe speed when compliance test  | 0: 2.5GT/s<br>1: 5GT/s        | 0                    |
| RSVD                | GPI08          | RESERVED  |                               | 0                    |
| BIF_VGA_DIS         | GPI09          | VGA ENABLED   |                               | 0                    |
| RSVD                | GPI021         | RESERVED  |                               | 0                    |
| BIOS_ROM_EN         | GPI0_22_ROMCSB | ENABLE EXTERNAL BIOS ROM  | 0: disable<br>1: enable       | X                    |
| ROMDCFG(2:0)        | GPI0(1:1:1)    | SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT  |                               | XXX                  |
| VP_DEVICE_STRAP_BNA | V2SYNC         | IGNORE VIP DEVICE STRAPS  |                               | 0                    |
| RSVD                | HSYNCR         |   |                               | 0                    |
| RSVD                | GENERIC        |   |                               | 0                    |
| ALD[1]              | HSYNCR         | ALD[1] ALD[0]<br>0: 0 No audio function<br>0: 1 Audio for DisplayPort and HDMI if dongle is detected<br>1: 0 Audio for DisplayPort only<br>1: 1 Audio for both DisplayPort and HDMI |                               | 11                   |
| ALD[0]              | VSYNCR         |   |                               |                      |

AMD RESERVED CONFIGURATION STRAPS  
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

| GPI021 | HSYNCR | GENERIC | GPI02 | GPI08 |
|--------|--------|---------|-------|-------|
|--------|--------|---------|-------|-------|

### STRAPS



### Internal VGA Thermal Sensor

Close to GPU

| Mars Pro MLPs | RV241 | RV242 | Bits [3:1] |
|---------------|-------|-------|------------|
| Hynix         | NC    | 4.75k | 000        |
| Samsung       | 8.45k | 2.7k  | 001        |
| Micron        | 4.75k | NC    | 111        |

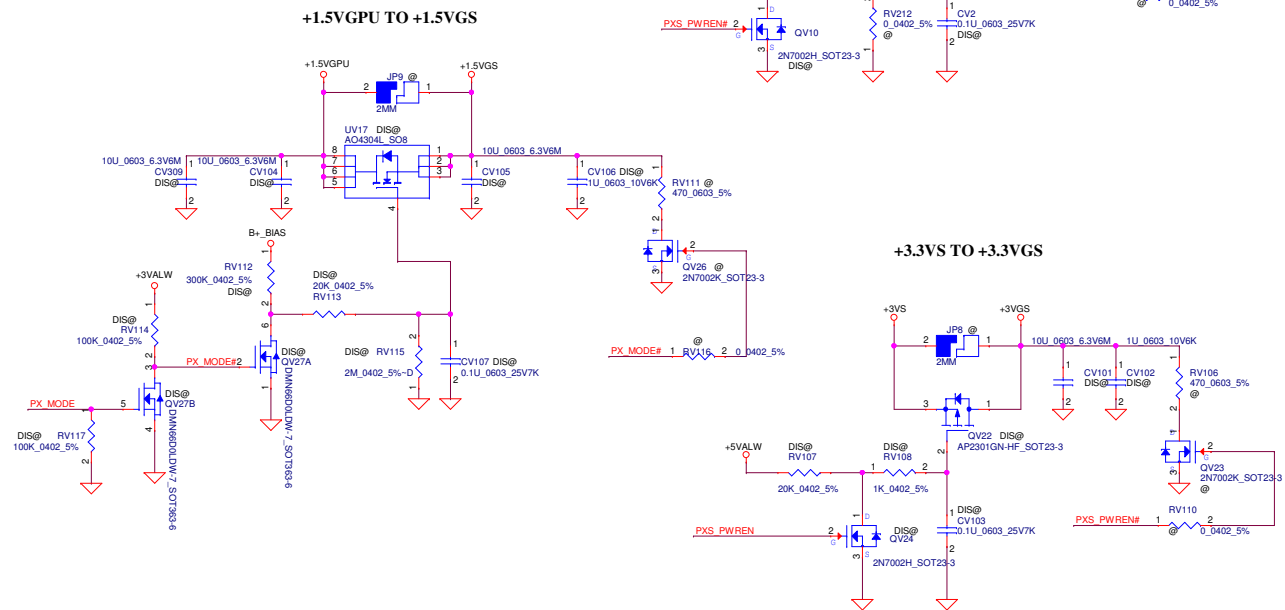
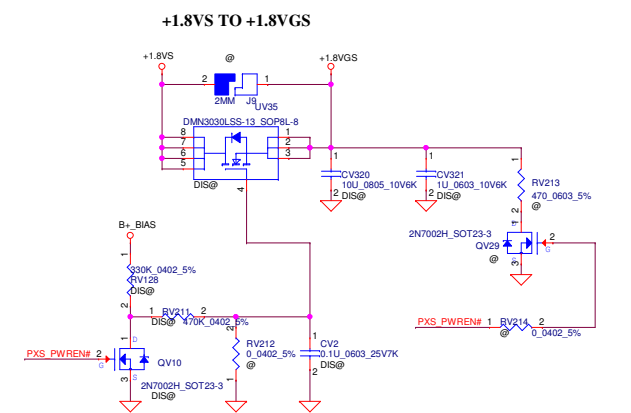
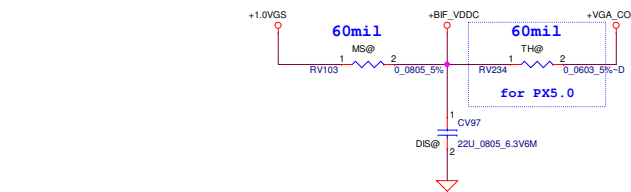
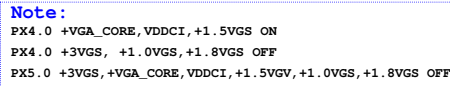
### VGA Thermal Sensor ADM1032ARMZ

Close to GPU

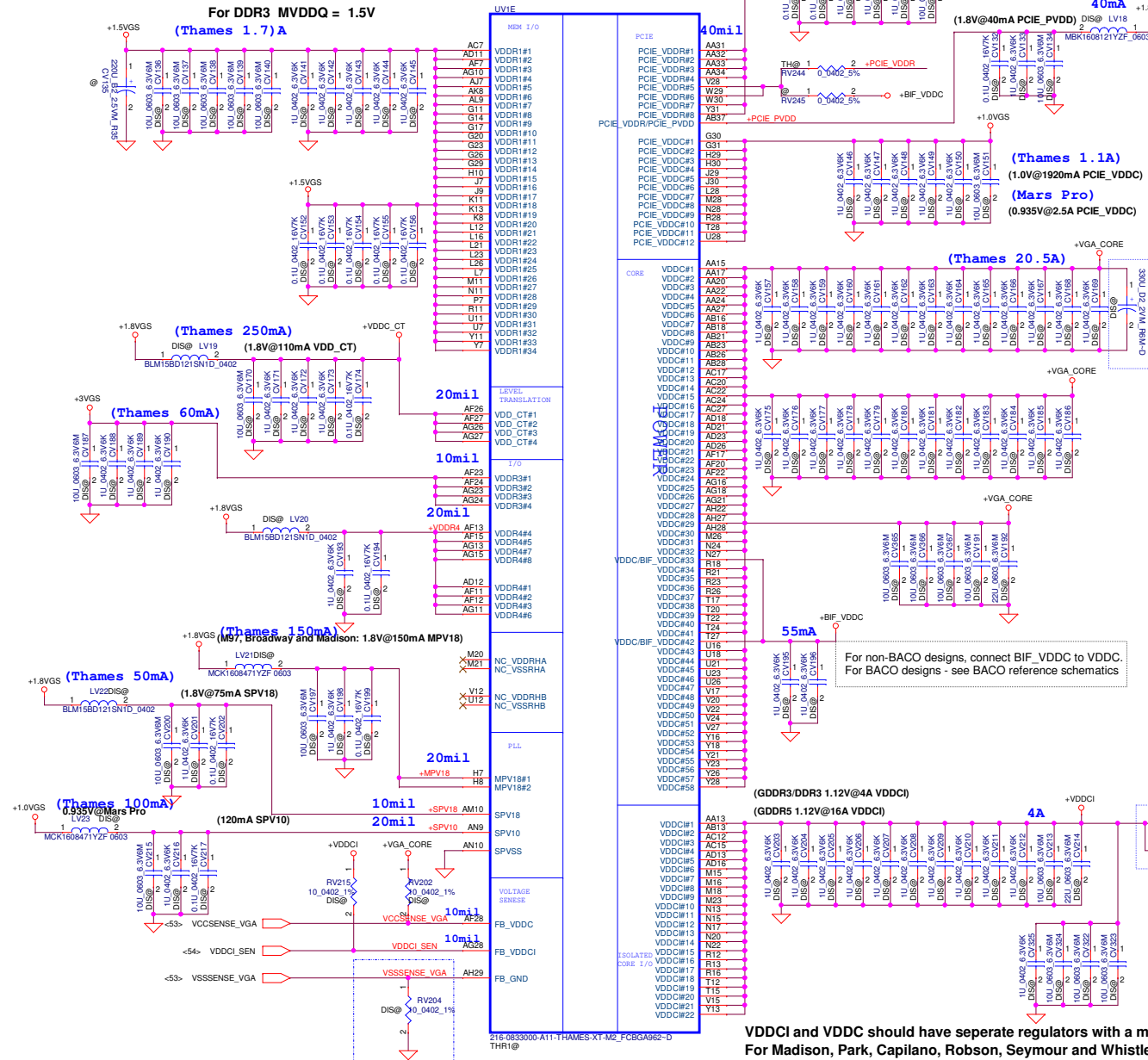
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| Security Classification   | Compal Secret Data |                 |            | Compal Electronics, Inc. |                            |                |
| Issued Date   | 2012/08/22         | Deciphered Date | 2013/08/31 | Title                    | ATI ThamesXT M2 BACO POWER |                |
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|   |                    |                 |            | Date:                    | Wednesday, August 29, 2012 | Sheet 26 of 57 |

Title: **ATI ThamesXT\_M2\_BACO POWER**  
 Size: Document Number: **LA-9101P** Rev: **0.4**  
 Date: **Wednesday, August 29, 2012** Sheet: **26** of **57**

## Power Sequence of Thames and Mars Pro



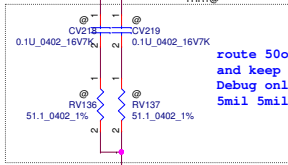




VDDCI and VDDC should have separate regulators with a merge option on PCB  
For Madison, Park, Capilano, Robson, Seymour and Whistler, VDDCI and VDDC can share one common regulator

|   |                            |                    |            |                          |          |
|---|----------------------------|--------------------|------------|--------------------------|----------|
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| Issued Date   | 2012/08/22                 | Deciphered Date    | 2013/08/31 | Title                    |          |
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|   |                            |                    |            | Doc Number               | LA-9101P |
| Date:   | Wednesday, August 28, 2012 |                    | Sheet      | 28                       | of 57    |

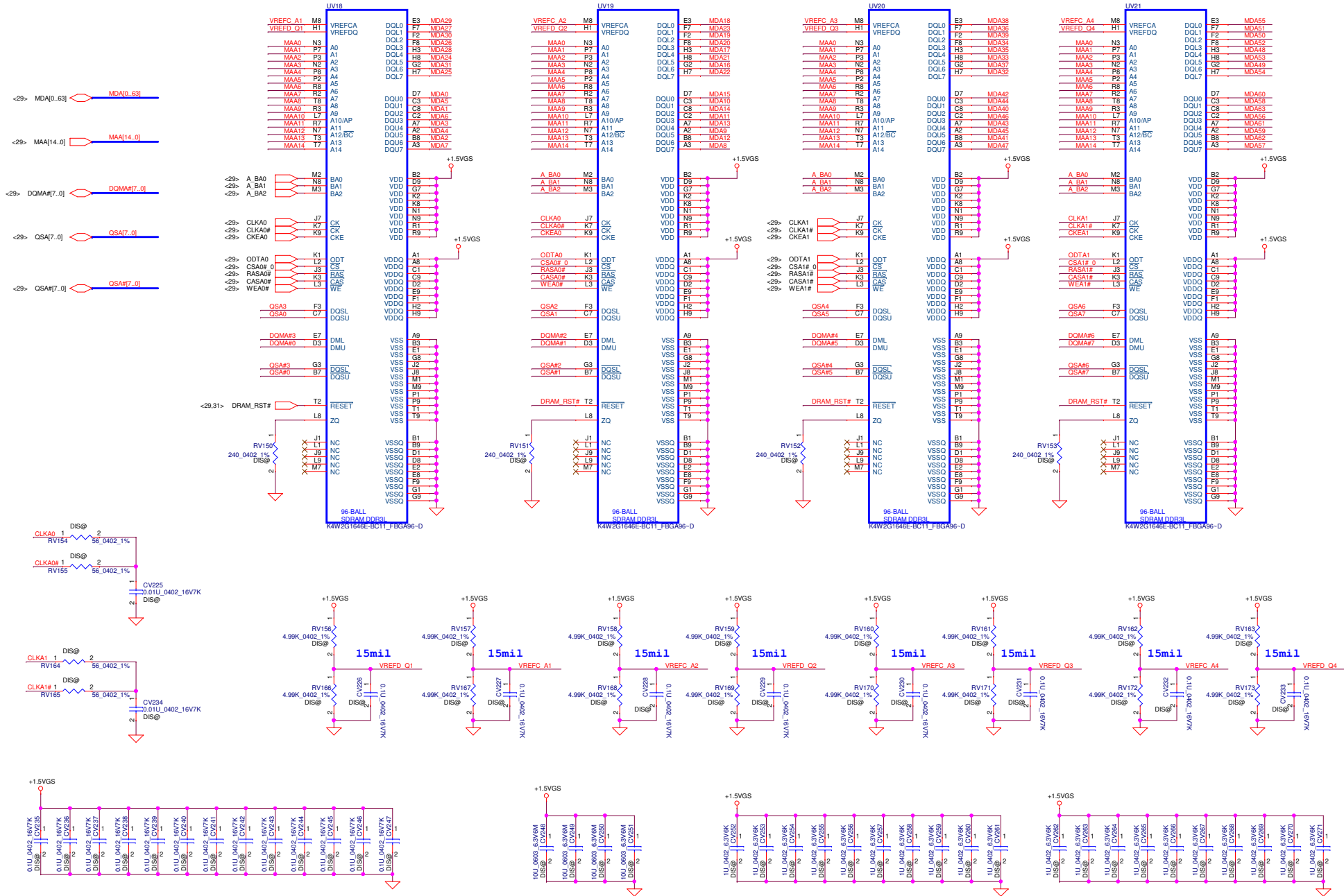




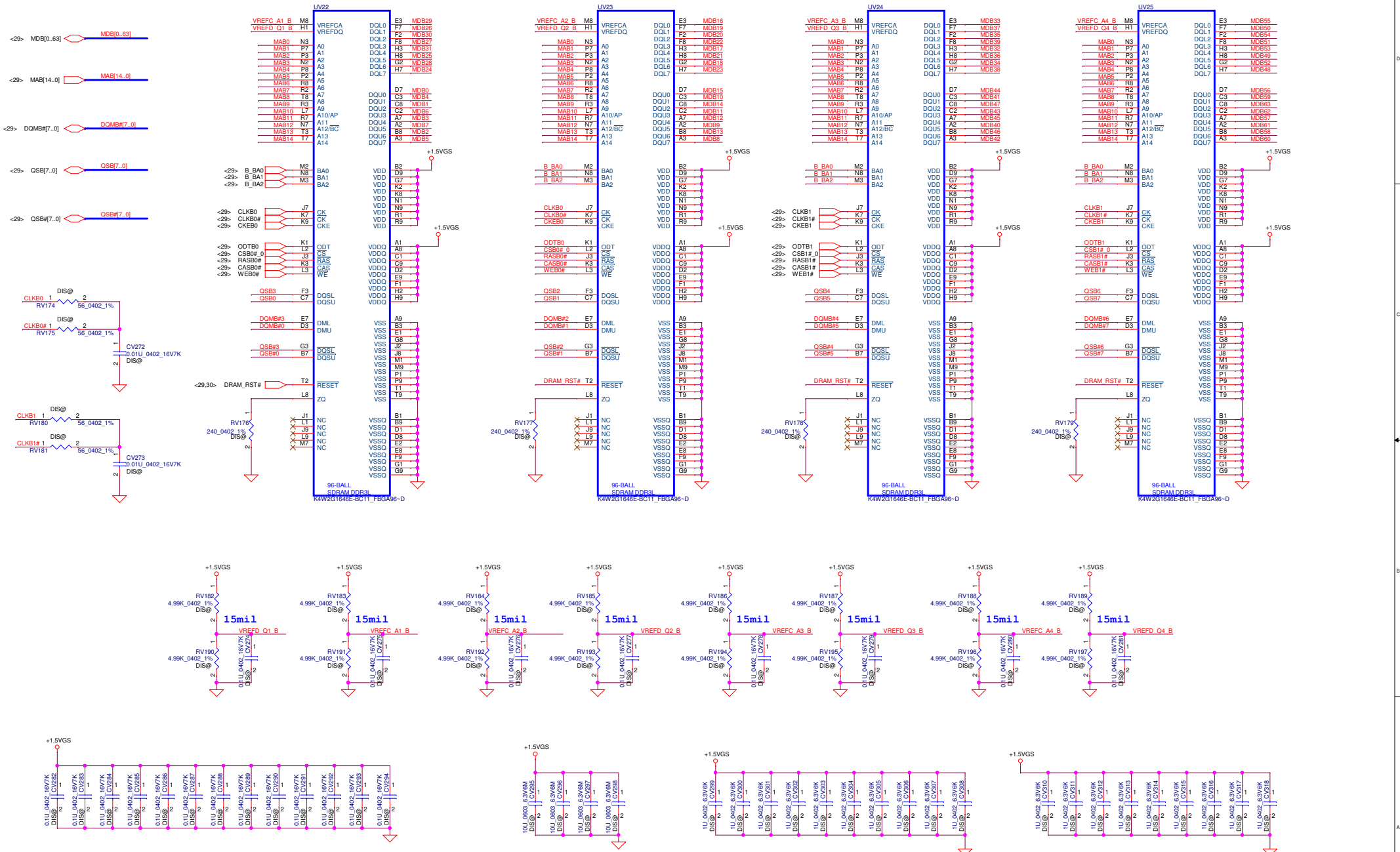
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| Security Classification   |  | Compal Secret Data |  | Compal Electronics, Inc. |                            |
| Issued Date   |  | 2012/08/22         |  | Deciphered Date          |                            |
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|   |  |                    |  | ATI ThamesXT M2 MEM IF   |                            |
|   |  |                    |  | Sheet                    | Document Number            |
|   |  |                    |  |                          | LA-9101P                   |
|   |  |                    |  | Date:                    | Wednesday, August 29, 2012 |
|   |  |                    |  | Sheet                    | 26 of 57                   |

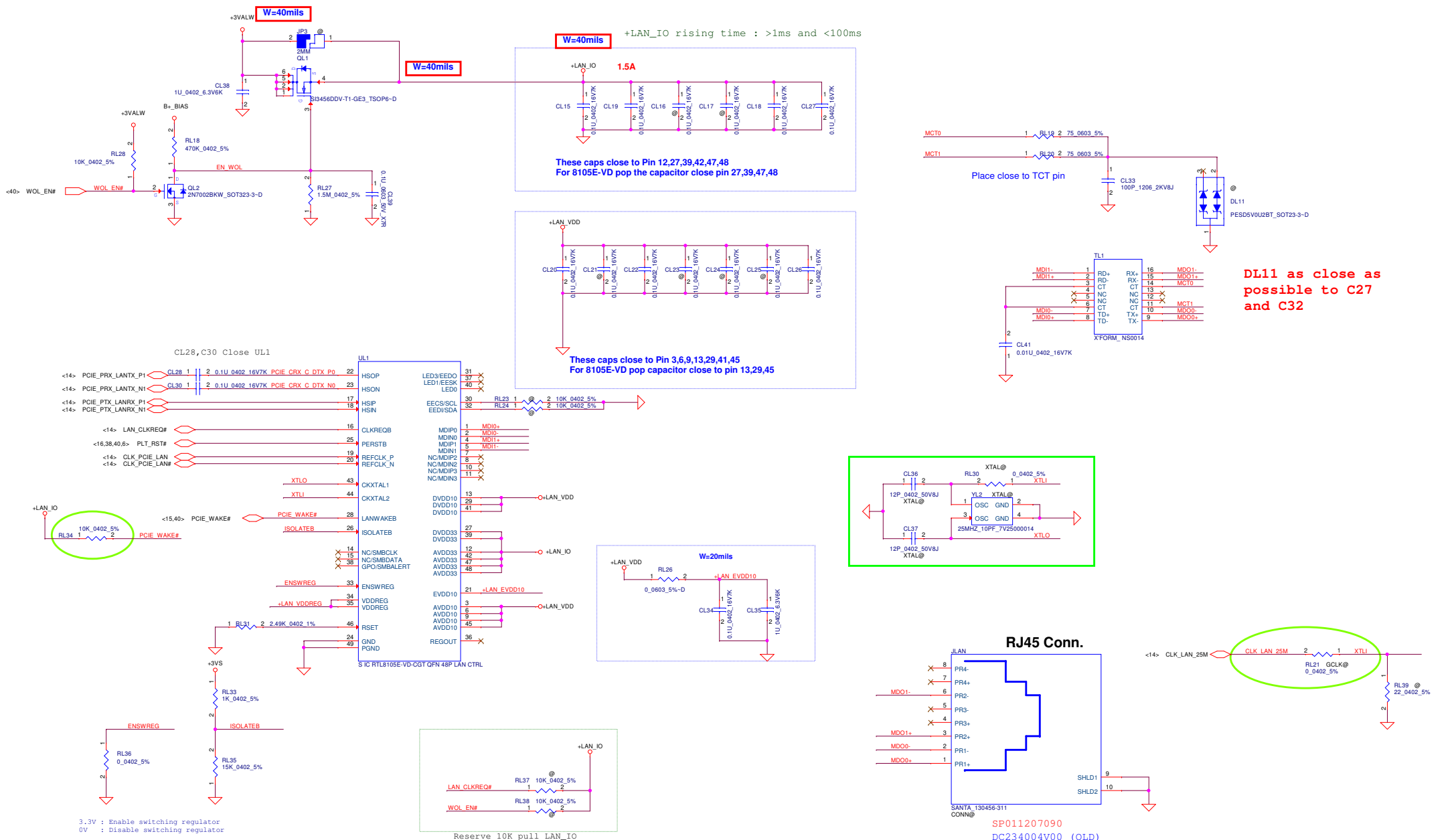


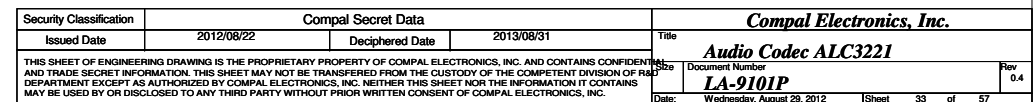
# CHANNEL A: 256MB/512MB DDR3

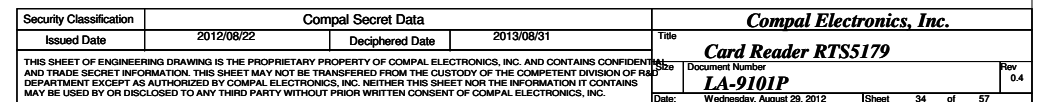


# CHANNEL B : 256MB/512MB DDR3

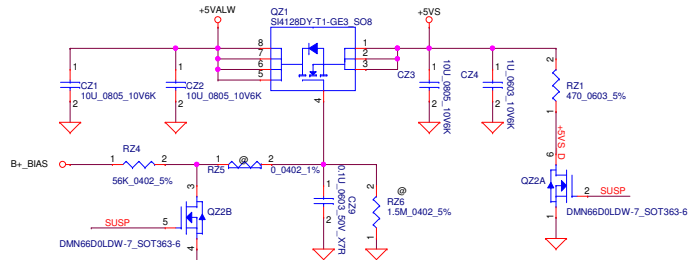




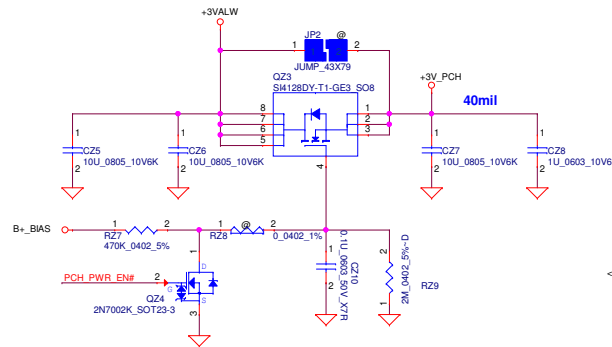




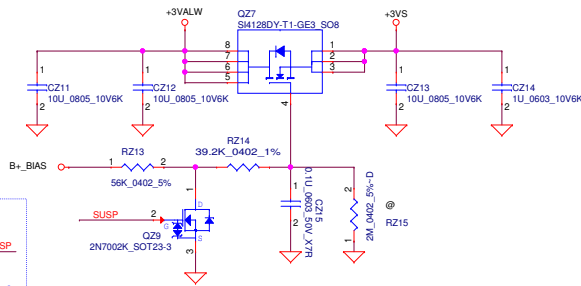
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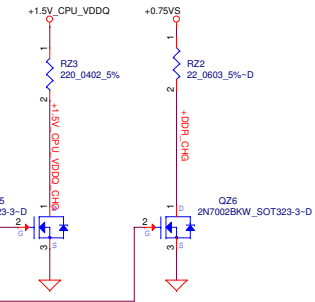
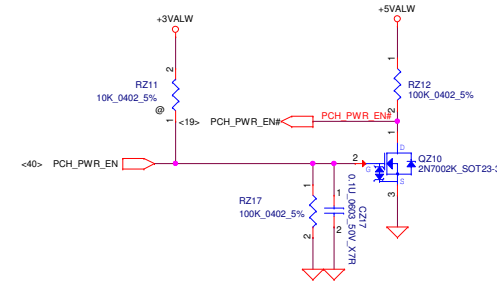
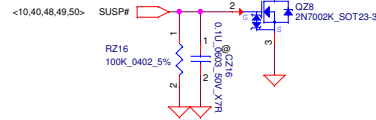
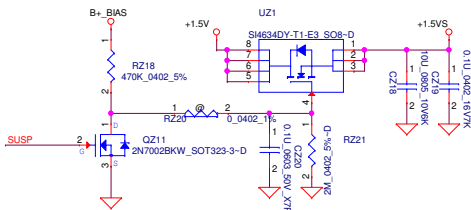
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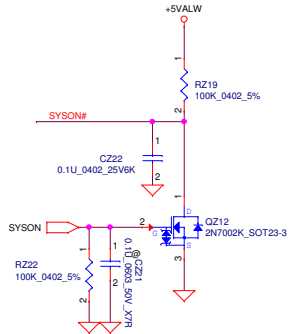
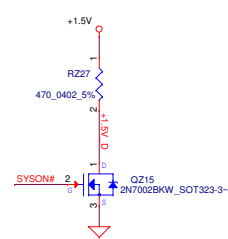
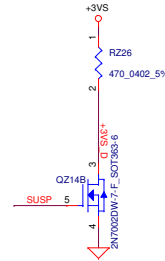
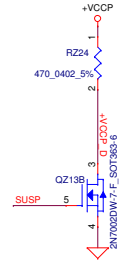
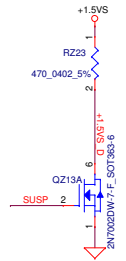
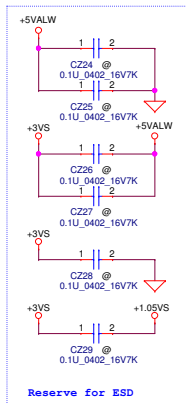
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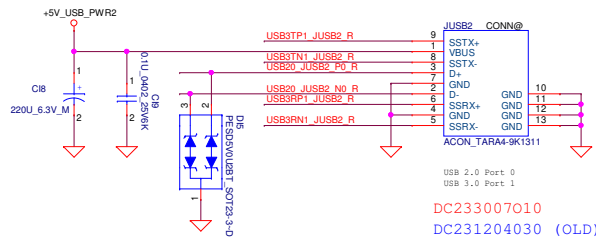
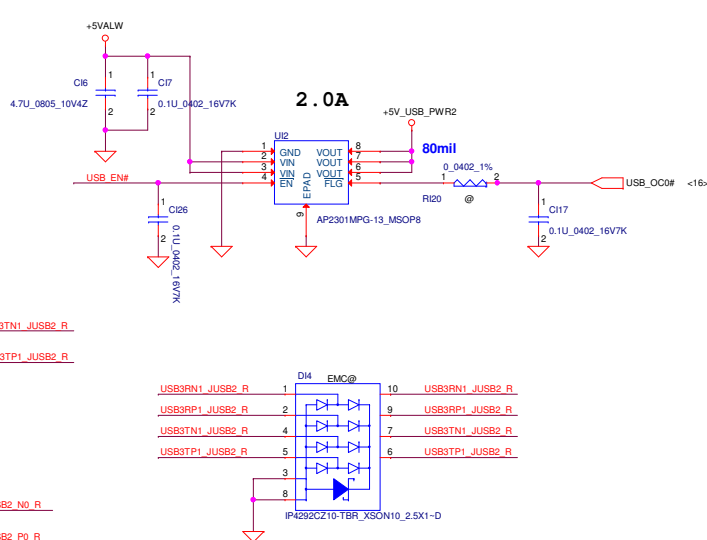
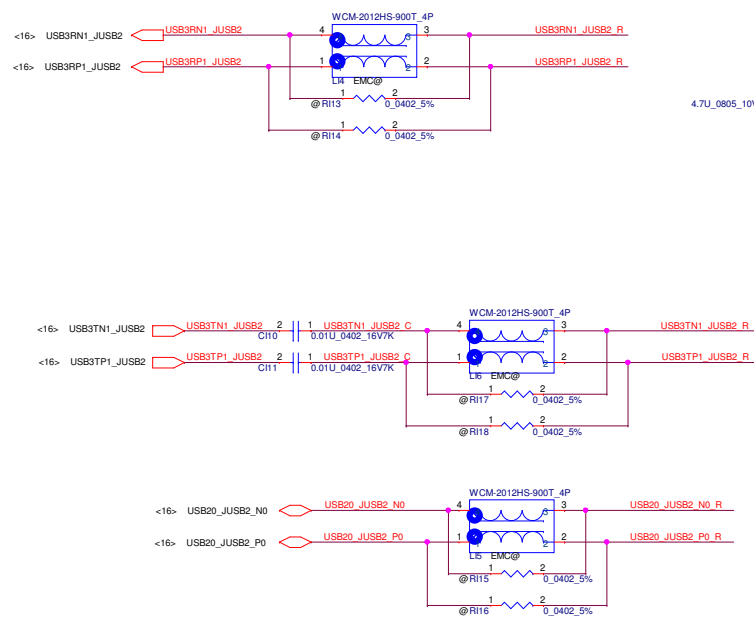
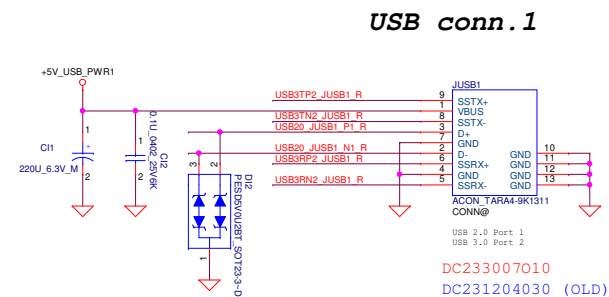
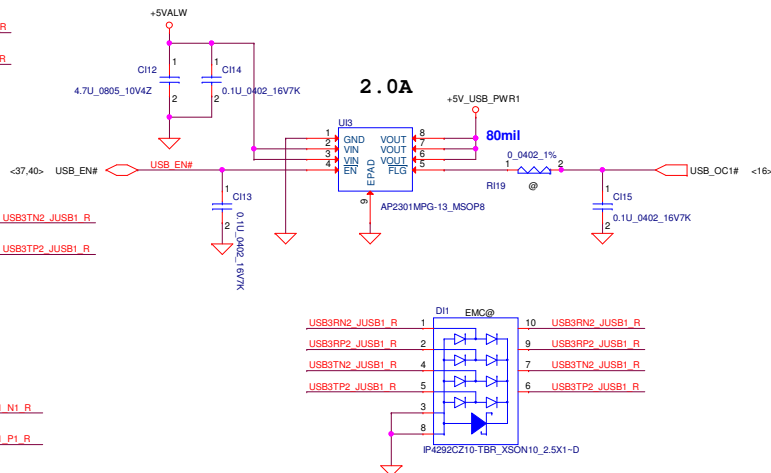
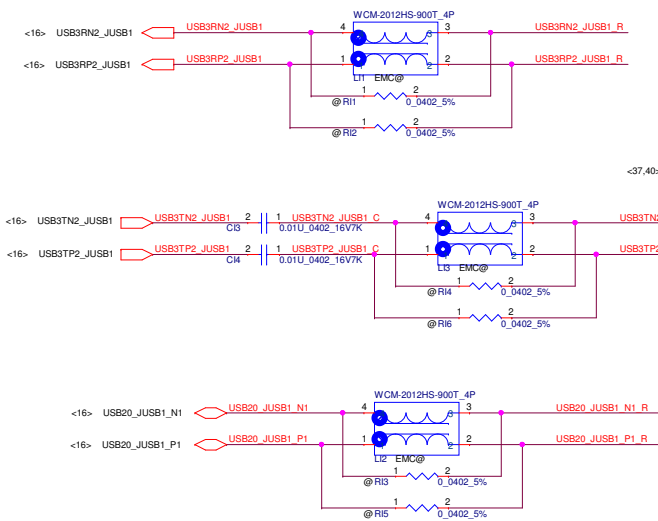
### +1.5V To +1.5VS



Reserve for ESD  
CZ23 2 1 SUSP  
0.1U\_0402\_16V7K  
Please close to Q29

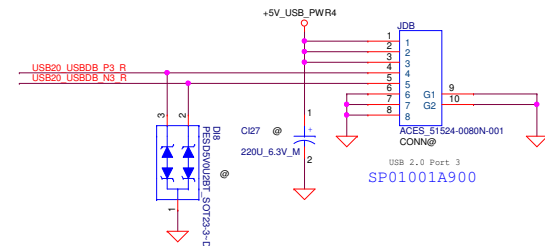
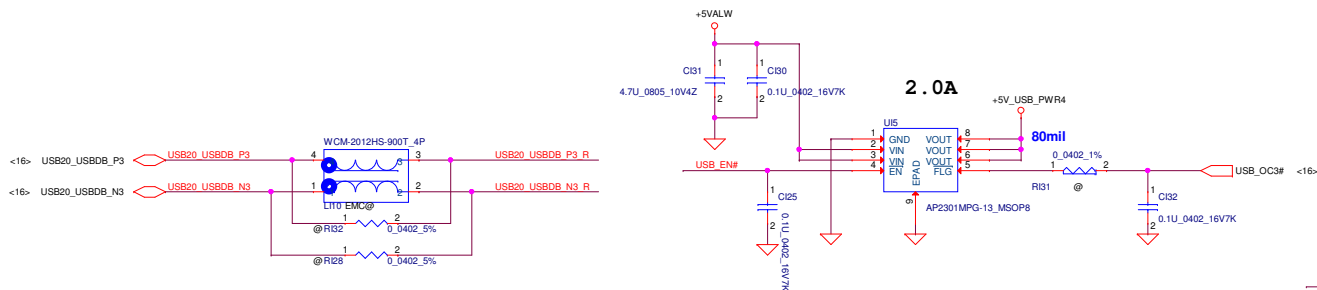
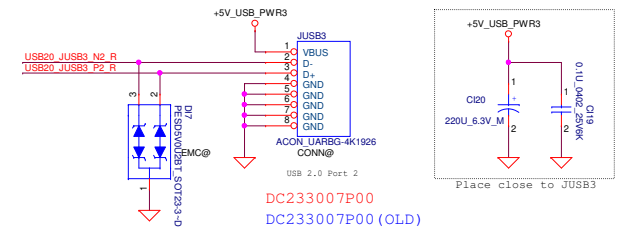
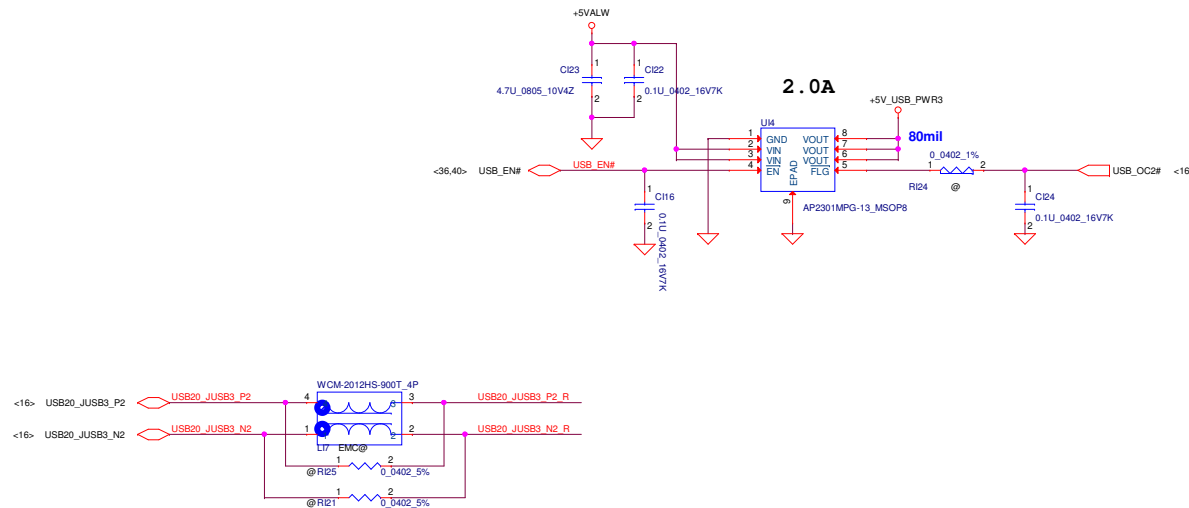


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| Security Classification   |  | Compal Secret Data |  | Title                      |  |
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| Sheet   |  | 35                 |  | of 57                      |  |

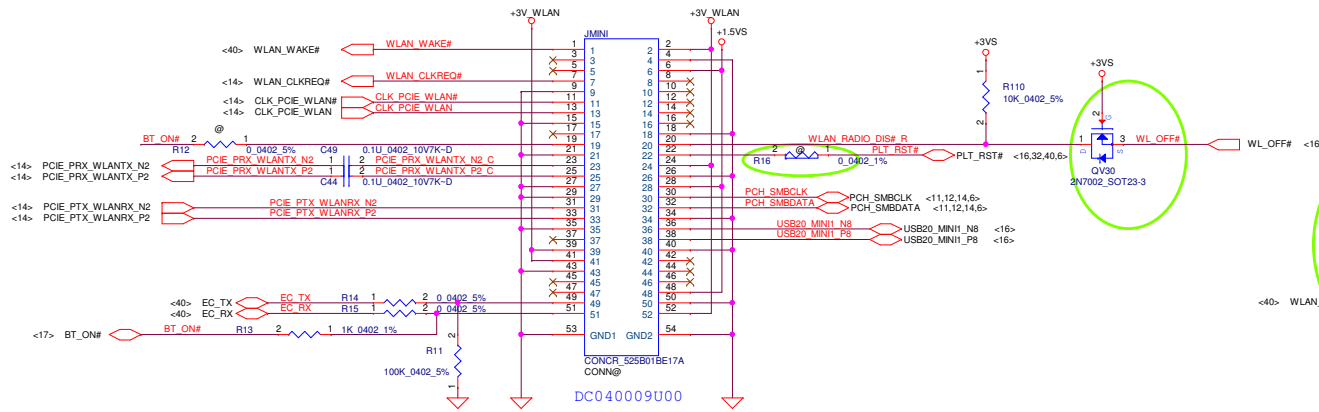


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| Issued Date   | 2012/08/22 | Deciphered Date    | 2013/08/31 | Document Number | USB3.0   |
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| Date: Wednesday, August 28, 2012  |            |                    |            | Sheet           | 36 of 57 |

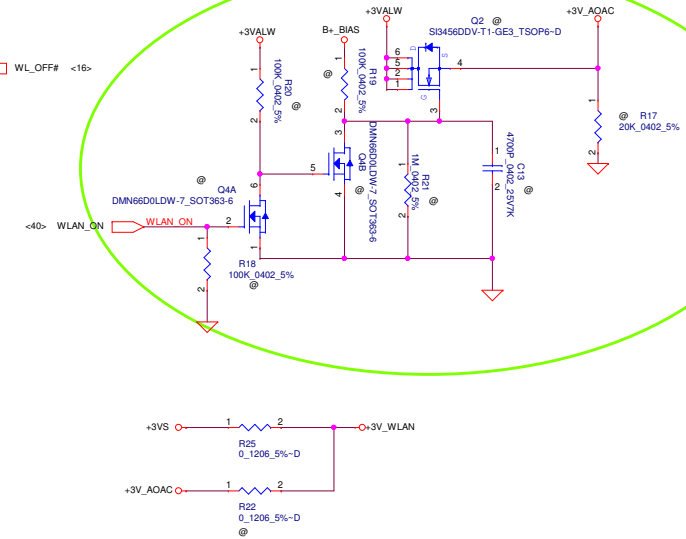




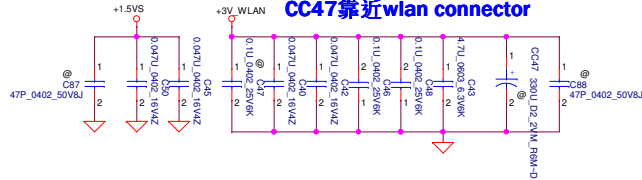
# Mini WLAN/WIMAX H=6.7



## Power Control for Mini Card



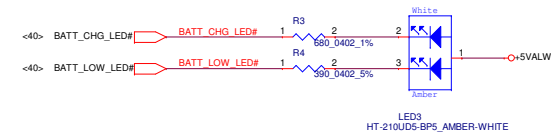
## CC47靠近wlan connector



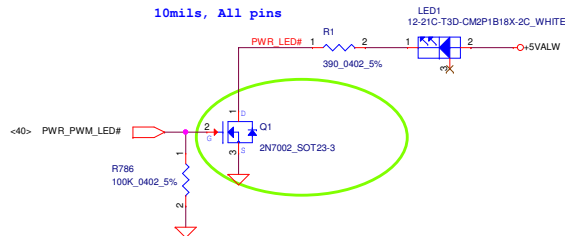
## HDD LED



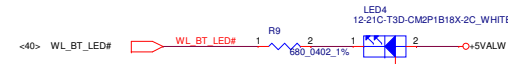
## Battery LED

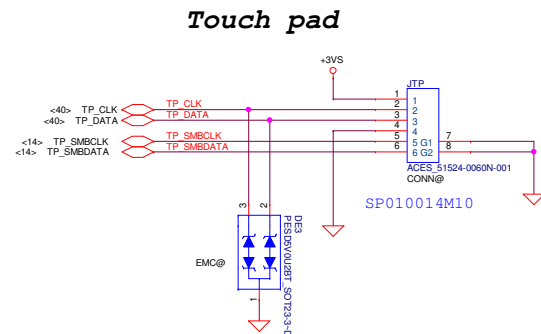
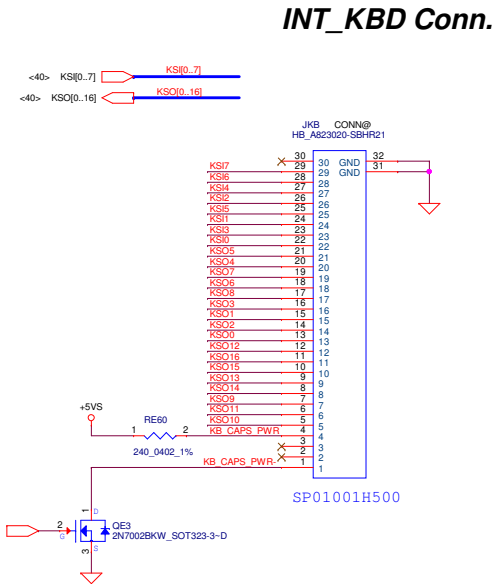
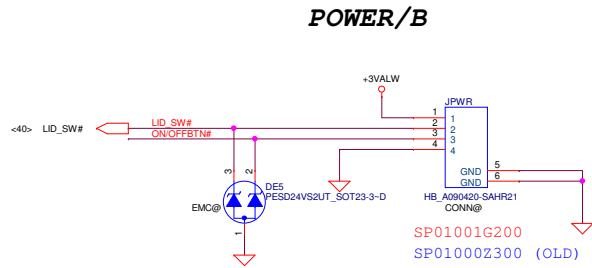
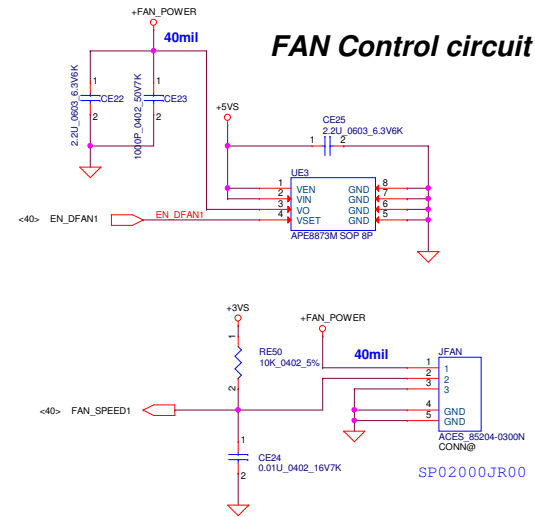
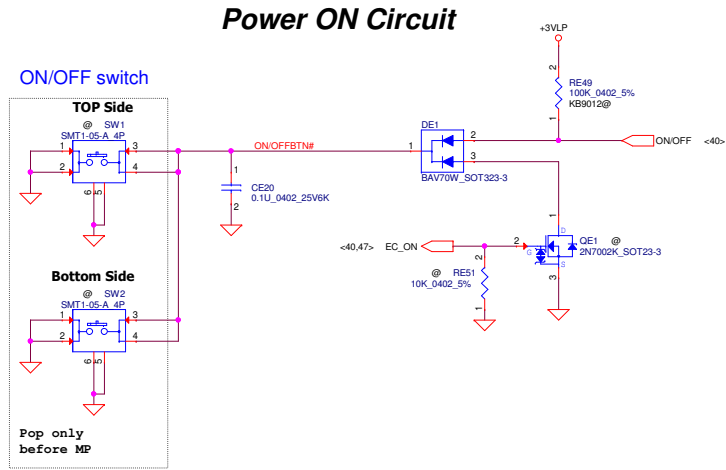


## Power LED



## Wireless LED



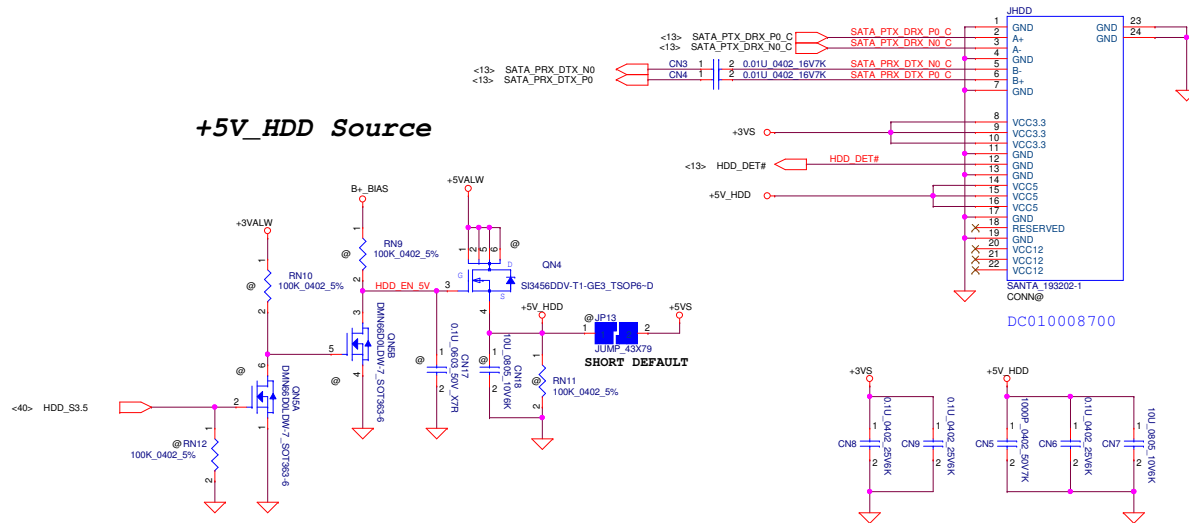


|   |            |                    |            |                 |                  |
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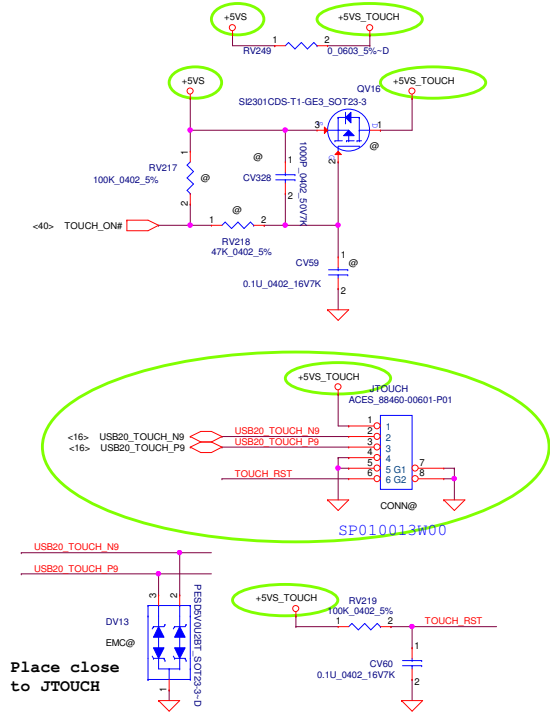


## SATA HDD Conn.

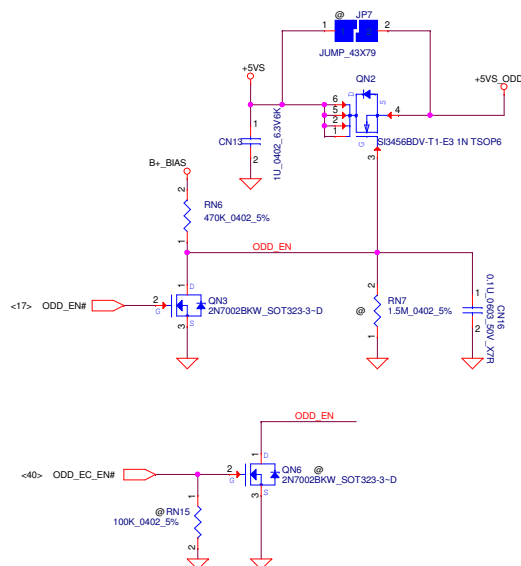
### +5V\_HDD Source



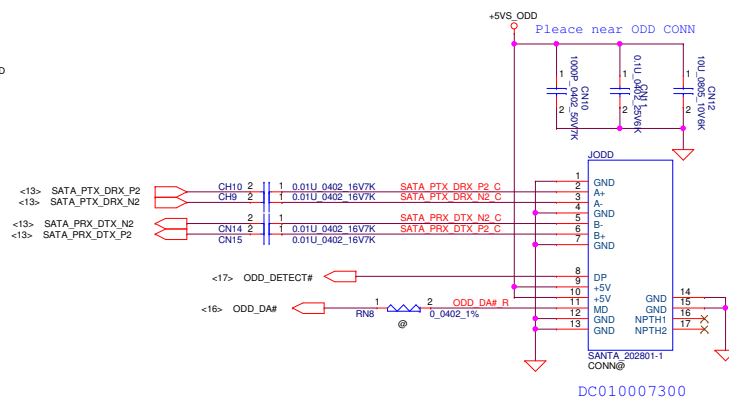
## \* Touch Screen Panel



### ODD Power Control

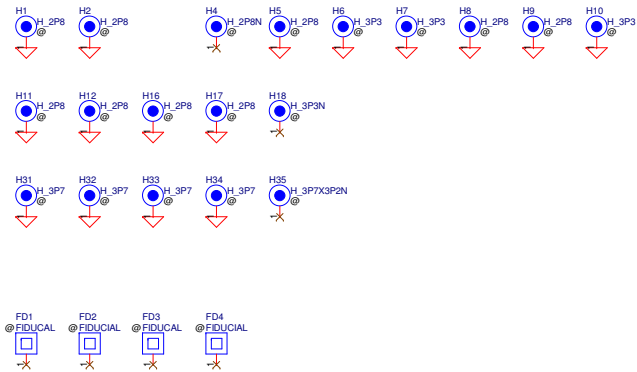


## SATA ODD Conn.



|   |            |                    |            |                 |          |
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Screw Hole



## Version Change List (P. I. R. List)

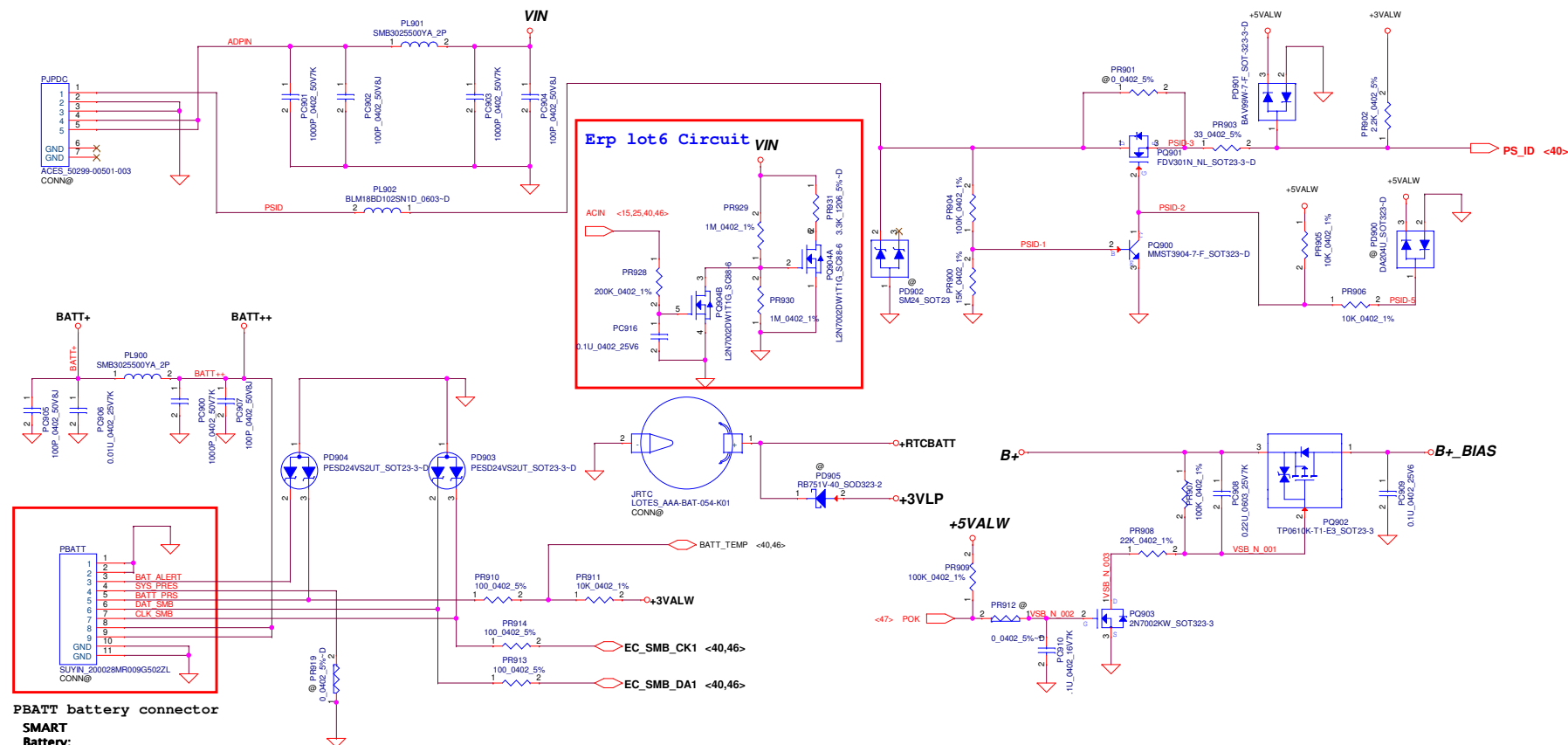
## Page 1

| Item | Page#                  | Title                 | Date       | Request Owner | Issue Description   | Solution Description   | Rev. |
|------|------------------------|-----------------------|------------|---------------|---|--|------|
| 1    | 34                     | Card Reader           | 2012/04/27 | HW            | The Card reader USB signal is incorrect.                      | SWAP UR1 USB signal P/N  | 0.2  |
| 2    | 40                     | Keyboard              | 2012/05/03 | SED           | Keyboard pin define change.                                   | Follow new SPEC.SWAP JKB pin define.   | 0.2  |
| 3    | 16, 21, 34, 36, 37, 38 | USB                   | 2012/05/04 | Function team | Change USB port assignment for function team request          | USB port change detail please reference Page.16 description.   | 0.2  |
| 4    | 26                     | VGA                   | 2012/05/05 | HW            | Delete reserve BACO circuit                                   | Delete UV15, QV16, QV17, QV18, QV19, QV20, RV99, RV100, RV249, CV96, CV98  | 0.2  |
| 5    | 42                     | DC/DC                 | 2012/05/07 | HW            | Design change   | UN-POP R211, POP R217  | 0.2  |
| 6    | 33                     | Audio codec           | 2012/05/09 | ESD           | ESD team ask solution   | Add RA29, RA30, RA31, RA32 and place on the moat between GND & GNDA  | 0.2  |
| 7    | 6, 17                  | PCH                   | 2012/05/09 | ESD           | ESD team ask reserve solution                                 | Add CC151, CH102 for reserve   | 0.2  |
| 8    | 32                     | LAN                   | 2012/05/10 | HW            | Remove China Go-rural for DELL request                        | Remove DL7, DL8, DL9   | 0.2  |
| 9    | 16, 38                 | USB                   | 2012/05/10 | HW            | Remove JUSB3 USB3.0   | Delete LI8, LI9, DI6 and change JUSB3 to USB2.0 type   | 0.2  |
| 10   | 32                     | Crystal               | 2012/05/15 | HW            | Crystal vendor suggestion                                     | Change CL36, CL37 from 33p/0402 to 12p/0402  | 0.2  |
| 11   | 21, 39                 | LVDS                  | 2012/05/17 | SED           | Add FHD Panel CE_ENABLE, DBC_ENABLE function from SED request | Add CE_EN, DBC_EN control pin to EC  | 0.2  |
| 12   | 21                     | LVDS                  | 2012/05/22 | SED           | Follow SED team request disable CE_EN function                | Change RV62 to DE-POP and RV100 to POP for disable CE_EN function  | 0.2  |
| 13   | 33                     | Audio codec           | 2012/05/23 | CODEC         | Follow CODEC vendor suggestion                                | Add AUDIO JACK PLUG delay circuit, Spearate NET JACK_PLUG to<br>-> JACK_SENSE# & "> JACK_PLUG#   | 0.2  |
| 14   | 16, 21                 | Touch Screen          | 2012/05/29 | HW            | Add touch screen function                                     | Add RV217, RV218, RV219, RV249, CV59, CV60, CV328, DV13, QV16, JTOUCH  | 0.2  |
| 15   | 39                     | Board ID              | 2012/05/30 | HW            | Board ID change for PT  | Change RE5 from 8.2k_0402(SD028820180) to 33k_0402(SD028330280)  | 0.2  |
| 16   | 21, 39                 | Touch Screen          | 2012/05/30 | HW            | Add touch screen function power control                       | Add NET "TOUCH_ON#" from JTOUCH to UE1.82(KB9012) for TOUCH SCREEN PANEL power control   | 0.2  |
| 17   | 33                     | Audio codec           | 2012/05/30 | HW            | Follow RealTek suggestion remove, delete reserve MUTE circuit | Delete D1, QA1, QA2, QA3, RA24, RA26, RA60, RA62, RA68, RA109, CA72, CA73  | 0.2  |
| 18   | 15, 16, 39, 41         | ESD                   | 2012/05/30 | ESD           | ESD ask CAP for reserve                                       | Reserve 0.1u/0402 CH104, CZ23, CH105, CE27, CE28   | 0.2  |
| 19   | 14                     | Green CLK             | 2012/05/30 | HW            | For Green CLK test  | Change RH31, RH41, RV232 0ohm form "GCLK#" to "g"<br>for break the clock signal to device  | 0.2  |
| 20   | 10, 26, 41             | DC/DC                 | 2012/05/31 | HW            | Change "+1.5V_CPU_VDDQ", "+1.5VS", "+1.5VGS" derating         | Change RC150 330K/0402 to 2M/0402, RC151 100K/0402 to 470K/0402, RZ18 100K/0402 to 470K/0402, RV115 0/0402 to 2M/0402  | 0.2  |
| 21   | 41                     | DC/DC                 | 2012/05/31 | HW            | For power sequence trunning                                   | Change RZ15 to DE-POP  | 0.2  |
| 22   | 06, 15, 16, 39, 41     | ESD                   | 2012/05/31 | ESD           | Follow ESD team request                                       | Change 0.1u/0402 from "g" to POP   | 0.2  |
| 23   | 32                     | Green CLK             | 2012/06/15 | HW            | Change for Green CLK bom control                              | Change RL21, RL30 from "g" to "GCLK#"  | 0.2  |
| 24   | 41                     | DC/DC                 | 2012/06/15 | HW            | For WLAN card power sequence issue                            | Change RZ4, RZ13 from 470K/0402 56K/0402   | 0.2  |
| 25   | 35, 41                 | Schematic page modify | 2012/06/18 | HW            | Schematic page modify for easily maintain.                    | Swap Page. 35 & Page 41.   | 0.2  |
| 26   | 41                     | ODD                   | 2012/06/18 | HW            | Change component location for easily maintain.                | Move RH42, RH43 from Page.13 to Page.41.   | 0.2  |
| 27   | 39                     | FAN                   | 2012/06/29 | HW            | Fan speed noise issue   | Reserve 220p/0402 CE24   | 0.3  |
| 28   | 6                      | CPU                   | 2012/06/29 | ESD           | System boot-up shot down issue.                               | Change CC151 from POP to "g"   | 0.3  |
| 29   | 21, 35, 39, 40, 41     | Circuit adjust        | 2012/07/01 | HW            | Circuit & page adjust for OAK 15" & OAK 17"                   | 1. Swap P.35 & P.41 and move touch screen circuit from P.21 to P.41.<br>2. Swap P.39 & P.40 page no  | 0.3  |
| 30   | 40                     | LID SW                | 2012/07/01 | HW            | LID SW need a trace for debug and switch.                     | Add RE81 for LID SW.   | 0.3  |
| 31   | 25                     | GPU                   | 2012/07/01 | HW            | Follow AMD request, MarsPro will used MPLs.                   | Change RV75, RV76, RV81 from "DIS#" to "TH#"   | 0.3  |
| 32   | 29                     | GPU                   | 2012/07/01 | HW            | Follow AMD request, MEM_CALRP2 is not need for Mars ASIC now. | Change RV205 from "MS#" to "g"   | 0.3  |
| 33   | 38                     | MINI card             | 2012/07/03 | HW            | Power Control for Mini card didn't need                       | Change R17 to "g"  | 0.3  |
| 34   | 6                      | XDP                   | 2012/07/06 | HW            | S3 return hang issue  | Change RC89 from "g" to POP  | 0.3  |
| 35   | 23                     | GREEN CLK             | 2012/07/09 | HW            | Follow Green CLK FAE suggestion                               | 1. Change UG1.2(+3VLP) & UG1.8(+3VALN) connect to +LAN_IO<br>2. Add R787 connect from +RTCBATT to C5.2 & UG1.10<br>3. Change C14 from 0.1u to 5p/0402<br>4. Change C8 connect from +3V_ALW to +LAN_IO<br>5. Add R788 0ohm/0402 from +RTCVCC to UG1 for GCLK & DH1 select | 0.3  |
| 36   | 35                     | MOAT                  | 2012/07/09 | ESD           | For ESD request reserve CAP.                                  | Reserve those CAP for ESD MOAT.  | 0.3  |
| 37   | 18                     | LVDS                  | 2012/07/10 | HW            | Change RES and reserve CAP for LVDS issue                     | Change RH185 from 0ohm-short to 0ohm/0805, and reserve CH106 1U/0402   | 0.3  |
| 38   | 41                     | Connector             | 2012/07/10 | ME            | For ME request  | Change JBTB1 footprint from SP02000G800 (OLD) to SP02000MJ00   | 0.3  |
| 39   | 13                     | PCH                   | 2012/07/11 | ESD           | Follow ESD team request                                       | Add RH44, RH48, RH70 & NET PCH_JTAG_TMS_R, PCH_JTAG_TDI_R, PCH_JTAG_IDO_R for break signal trace   | 0.3  |
| 40   | 40                     | PCH                   | 2012/07/11 | ESD           | Follow ESD team request                                       | 1. Change NET NAME "N59110727" to "WL_BT_LED#_R"<br>2. Reserve 0.1u/0402 on "WL_BT_LED#_R" for ESD   | 0.3  |
| 41   | 21                     | LVDS                  | 2012/07/11 | HW            | Reserve for CE function for LVDS connector                    | Change CE_EN_R from dummy to JLVDS.18  | 0.3  |

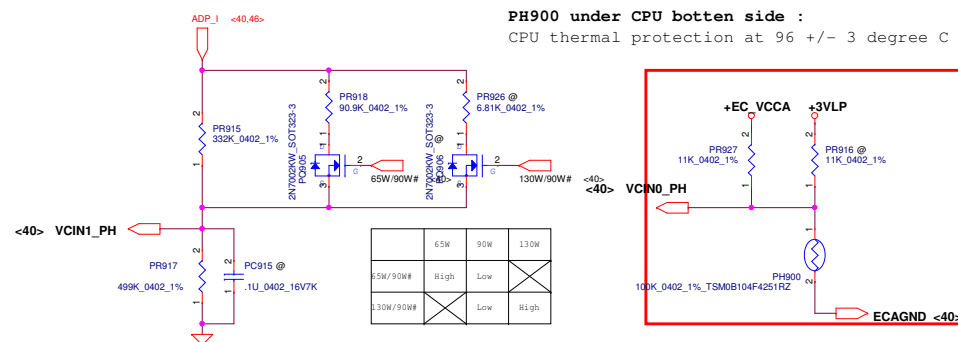
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|   |            |                    |            | Rev                      | 0.4                        |

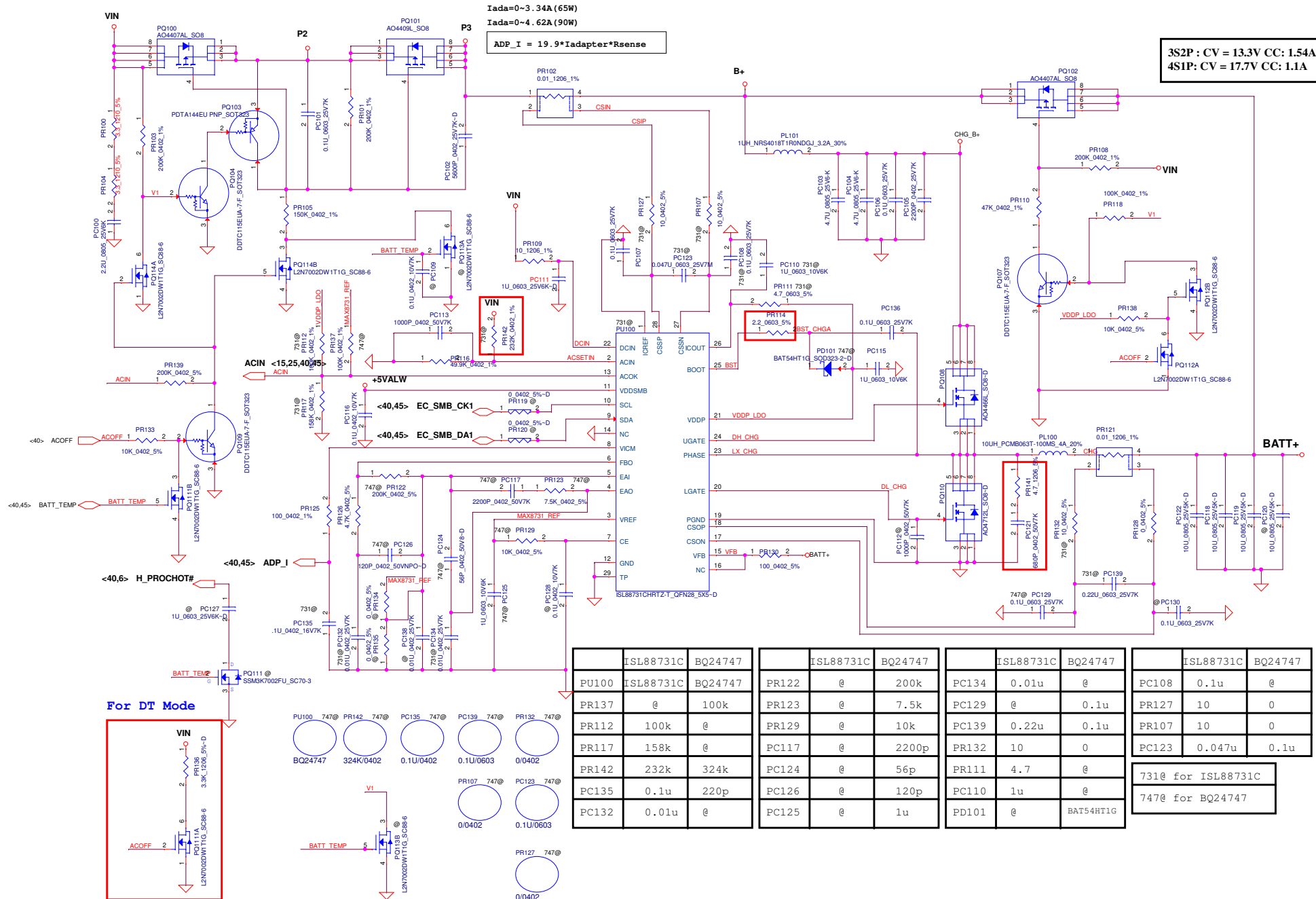


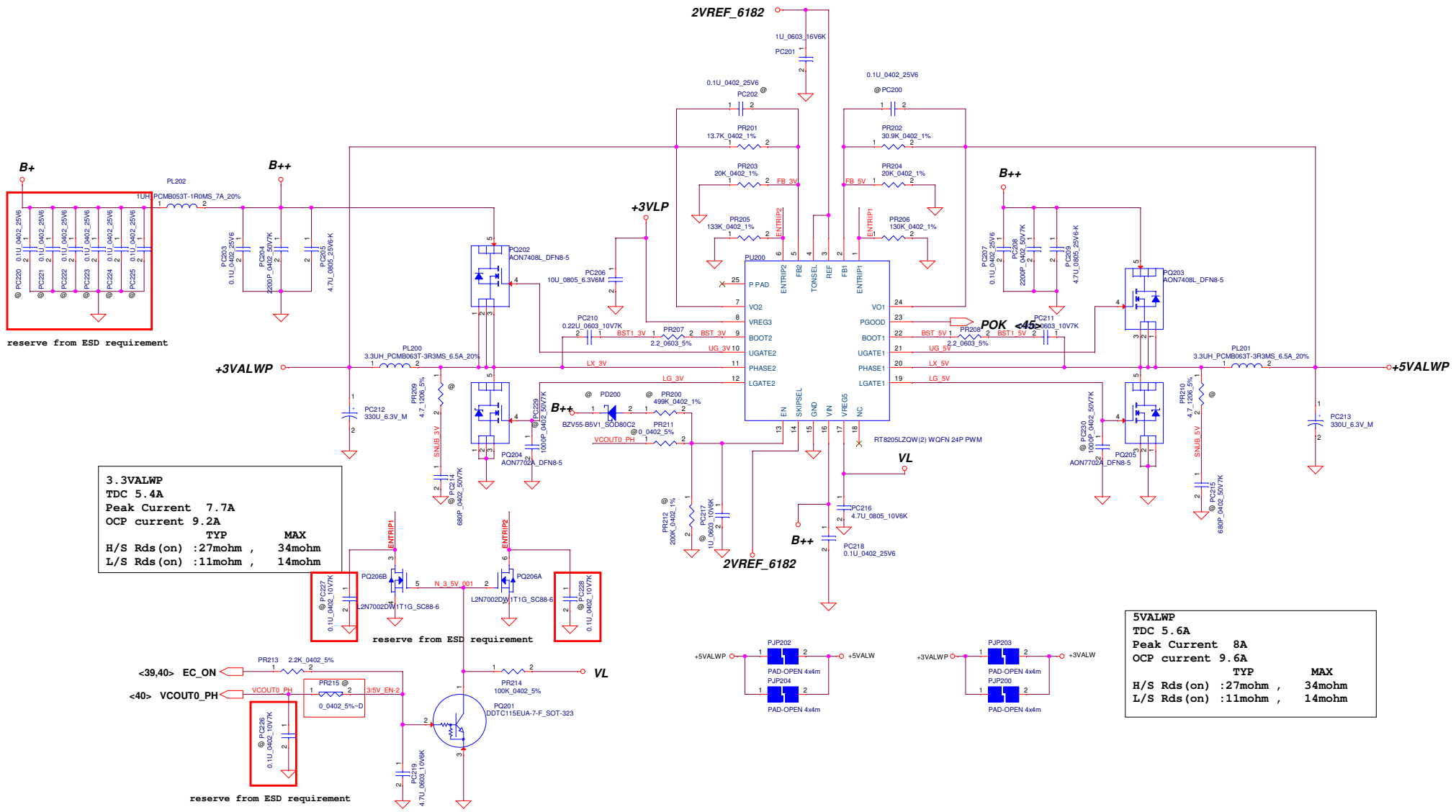
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PH900 under CPU bottom side :  
CPU thermal protection at 96 +/- 3 degree C





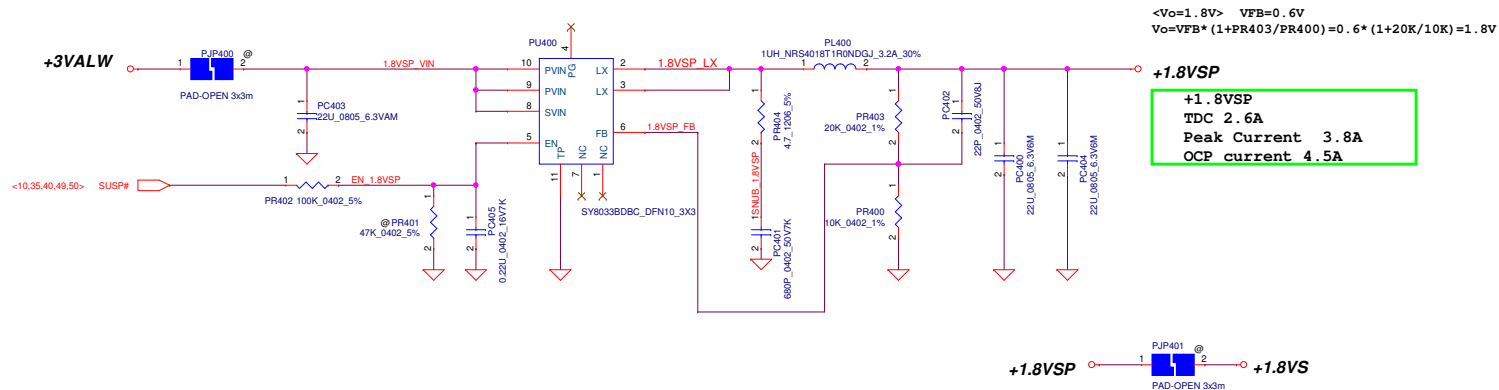


**3.3VALWP**  
TDC 5.4A  
Peak Current 7.7A  
OCP current 9.2A  
TYP  
H/S Rds (on) : 27mohm , 34mohm  
L/S Rds (on) : 11mohm , 14mohm

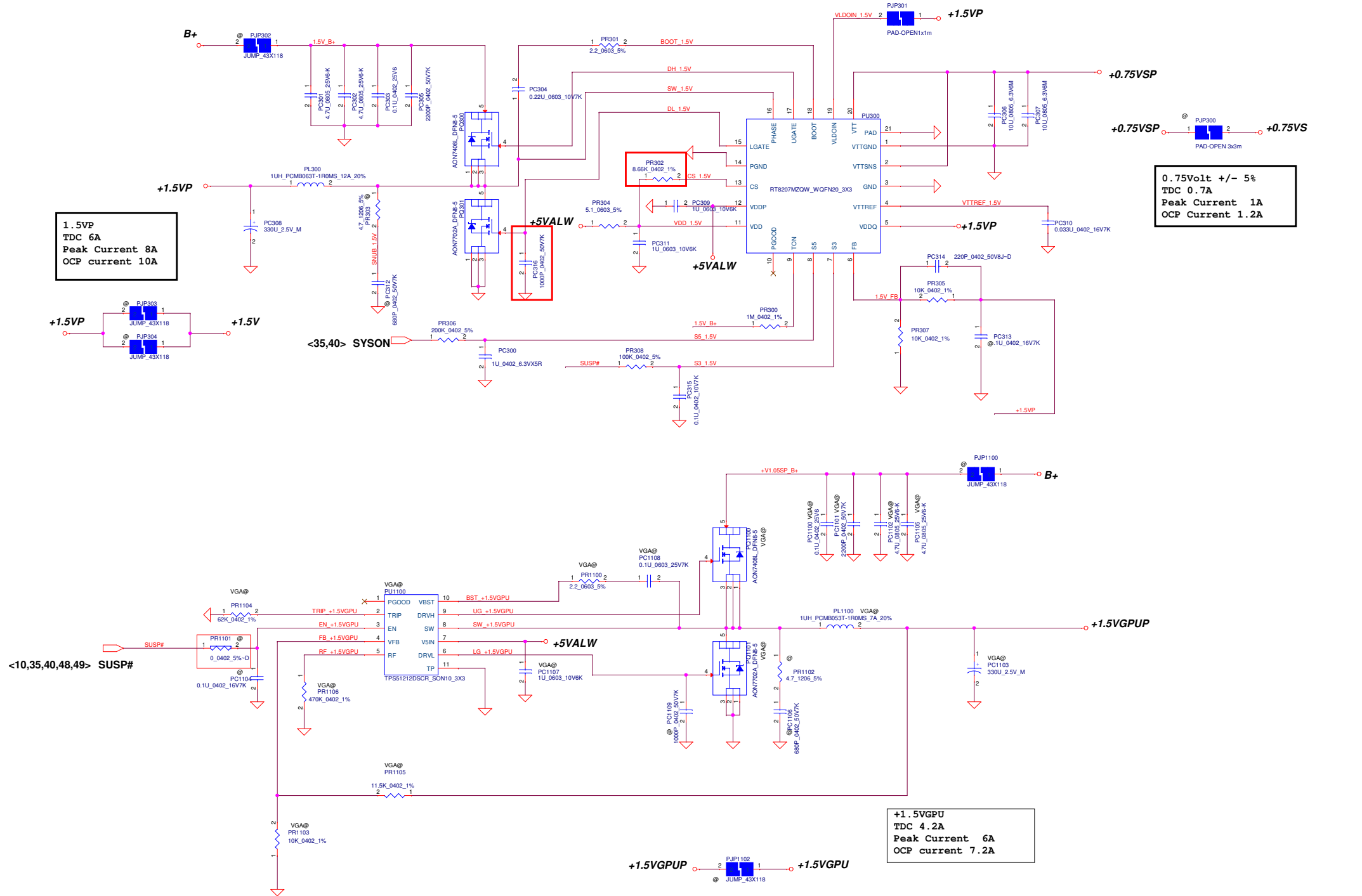
**5VALWP**  
TDC 5.6A  
Peak Current 8A  
OCP current 9.6A  
TYP  
H/S Rds (on) : 27mohm , 34mohm  
L/S Rds (on) : 11mohm , 14mohm

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|   |  |                    |  |                            |  |
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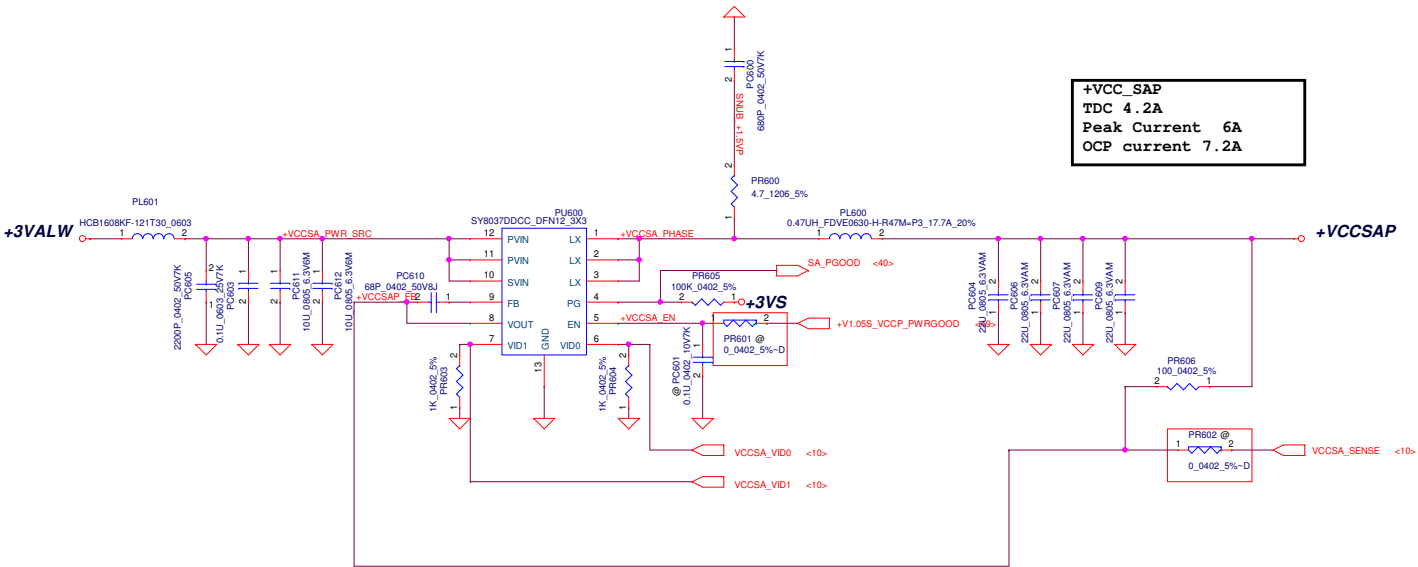






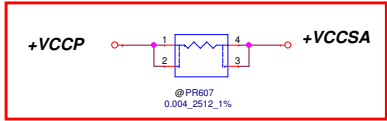
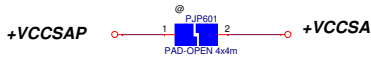
| VID [0] | VID[1] | VCCSA Vout |
|---------|--------|------------|
| 0       | 0      | 0.9V       |
| 0       | 1      | 0.85V      |
| 1       | 0      | 0.775V     |
| 1       | 1      | 0.75V      |

output voltage adjustable network



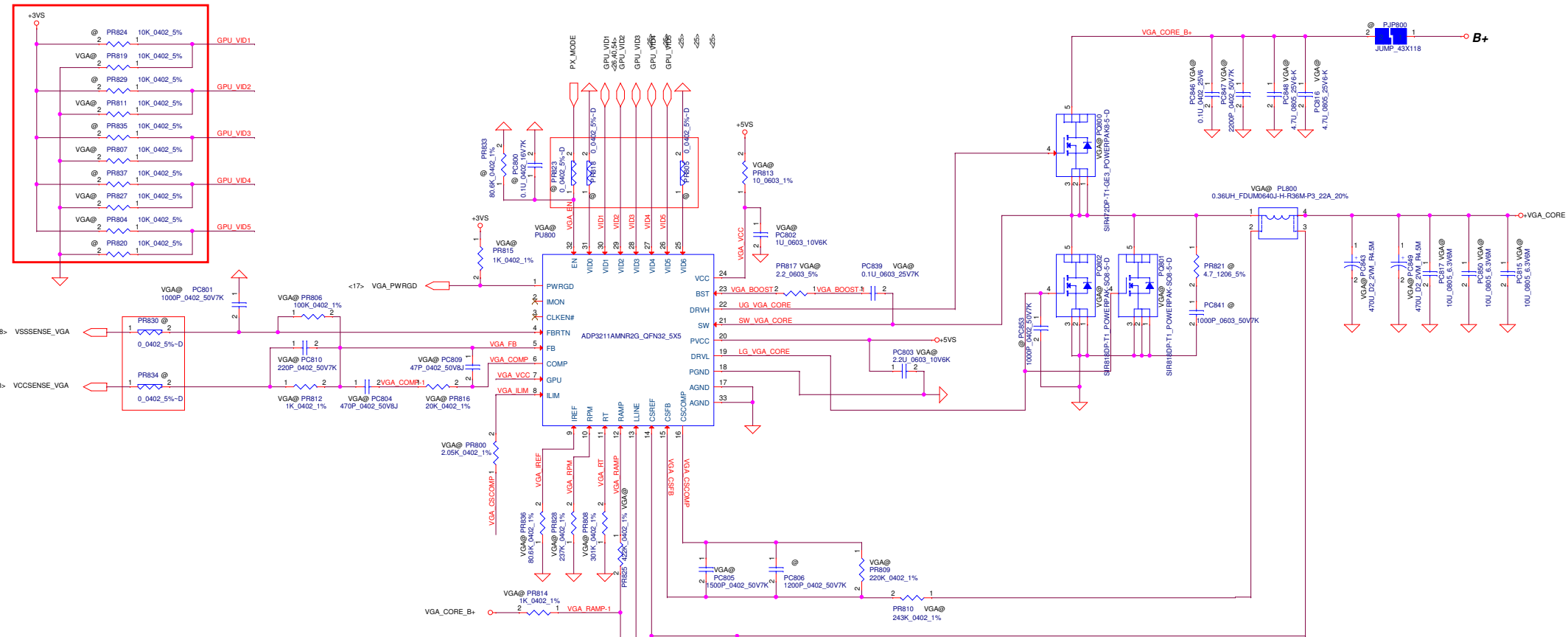
**+VCC\_SAP**  
TDC 4.2A  
Peak Current 6A  
OCP current 7.2A

The 1k PD on the VCCSA VIDs are empty.  
These should be stuffed to ensure that  
VCCSA VID is 00 prior to VCCIO stability.



reserve for Pentium and Celeron only





Mars Pro

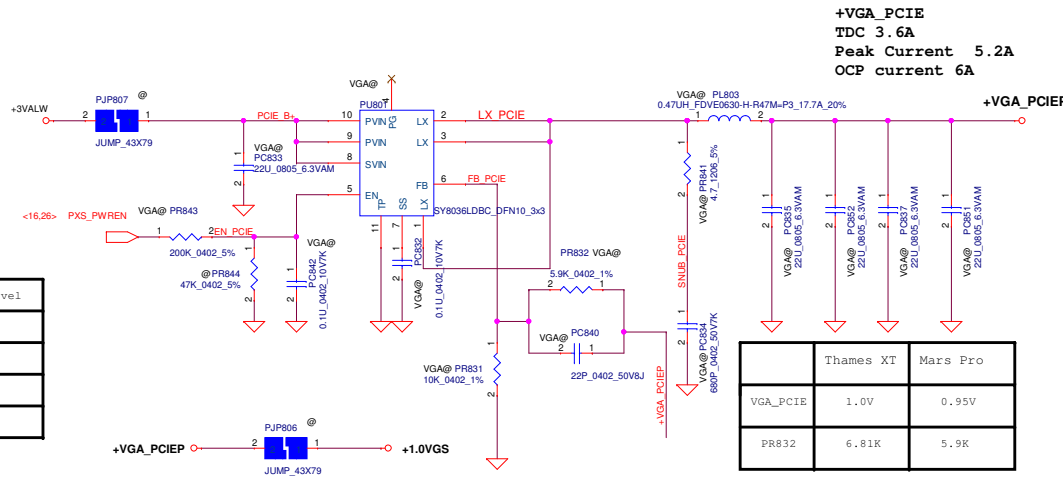
| GPU_VID5<br>(GPIO_10) | GPU_VID4<br>(GPIO_14) | GPU_VID3<br>(GPIO_15) | GPU_VID2<br>(GPIO_16) | GPU_VID1<br>(GPIO_20) | Core Voltage Level |
|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|--------------------|
| 0                     | 1                     | 1                     | 1                     | 1                     | 1.125V             |
| 1                     | 0                     | 0                     | 0                     | 0                     | 1.1V               |
| 1                     | 0                     | 0                     | 0                     | 1                     | 1.075V             |
| 1                     | 0                     | 0                     | 1                     | 0                     | 1.05V              |
| 1                     | 0                     | 0                     | 1                     | 1                     | 1.025V             |
| 1                     | 0                     | 1                     | 0                     | 0                     | 1V                 |
| 1                     | 0                     | 1                     | 0                     | 1                     | 0.975V             |
| 1                     | 0                     | 1                     | 1                     | 0                     | 0.95V              |
| 1                     | 0                     | 1                     | 1                     | 1                     | 0.925V             |
| 1                     | 1                     | 0                     | 0                     | 0                     | 0.9V               |
| 1                     | 1                     | 0                     | 0                     | 1                     | 0.875V             |
| 1                     | 1                     | 0                     | 1                     | 0                     | 0.85V              |
| 1                     | 1                     | 0                     | 1                     | 1                     | 0.825V             |
| 1                     | 1                     | 1                     | 0                     | 0                     | 0.8V               |

**+VGA\_CORE**  
TDC 22A  
Peak Current 30A  
OCP current 36A  
FSW=350kHz  
DCR 1.1mohm +/-5%  
Loadline = 1.5mohm

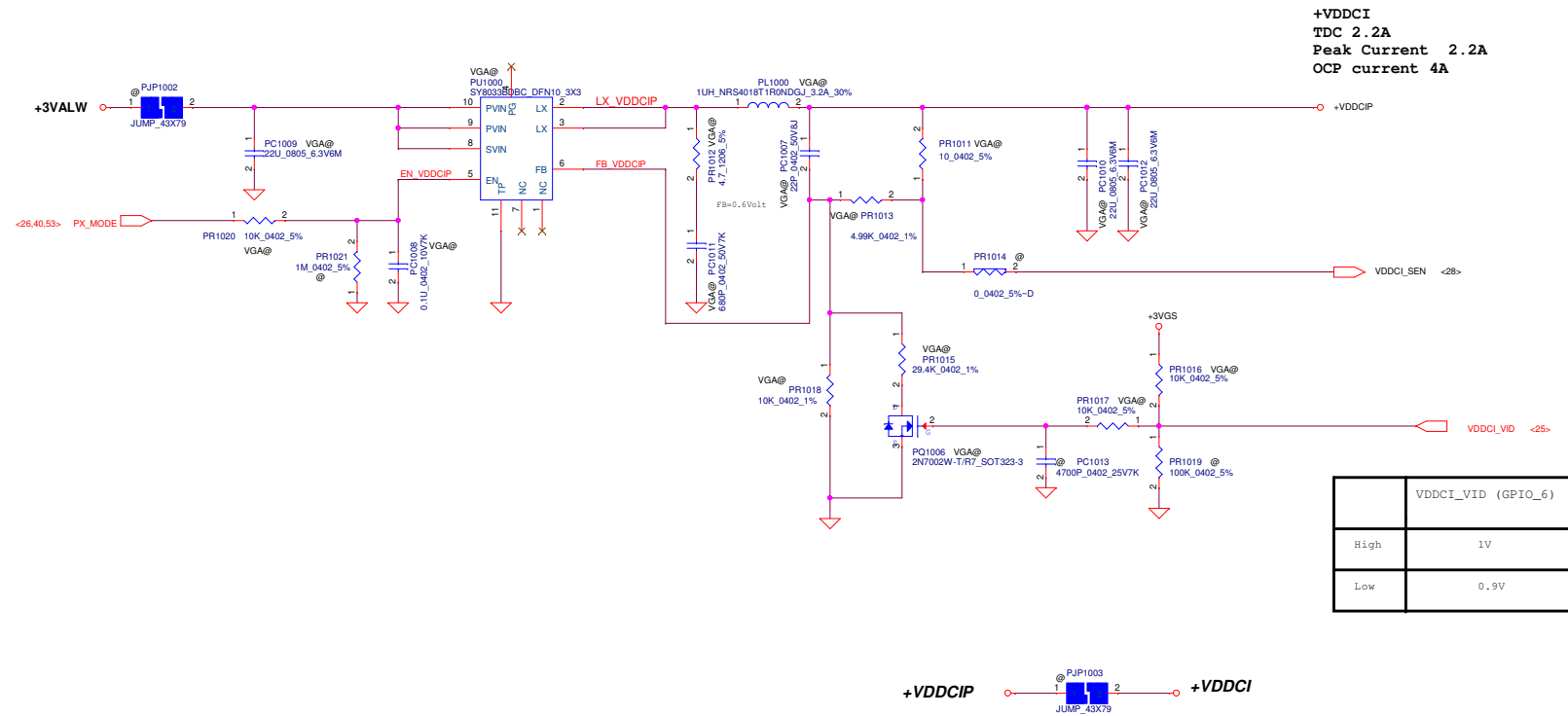
Thames XT

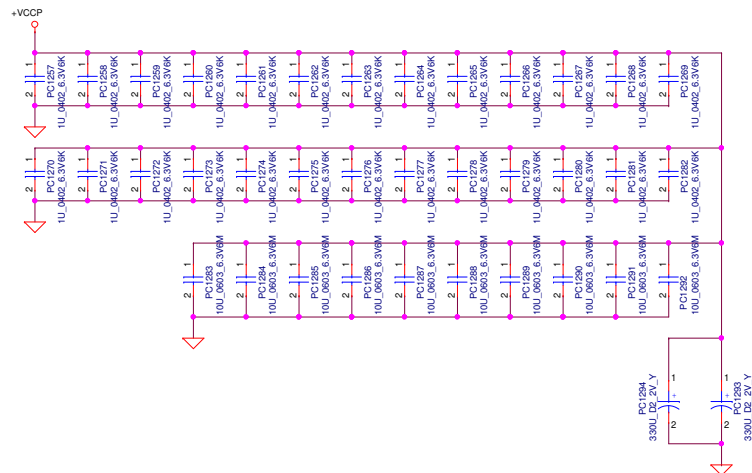
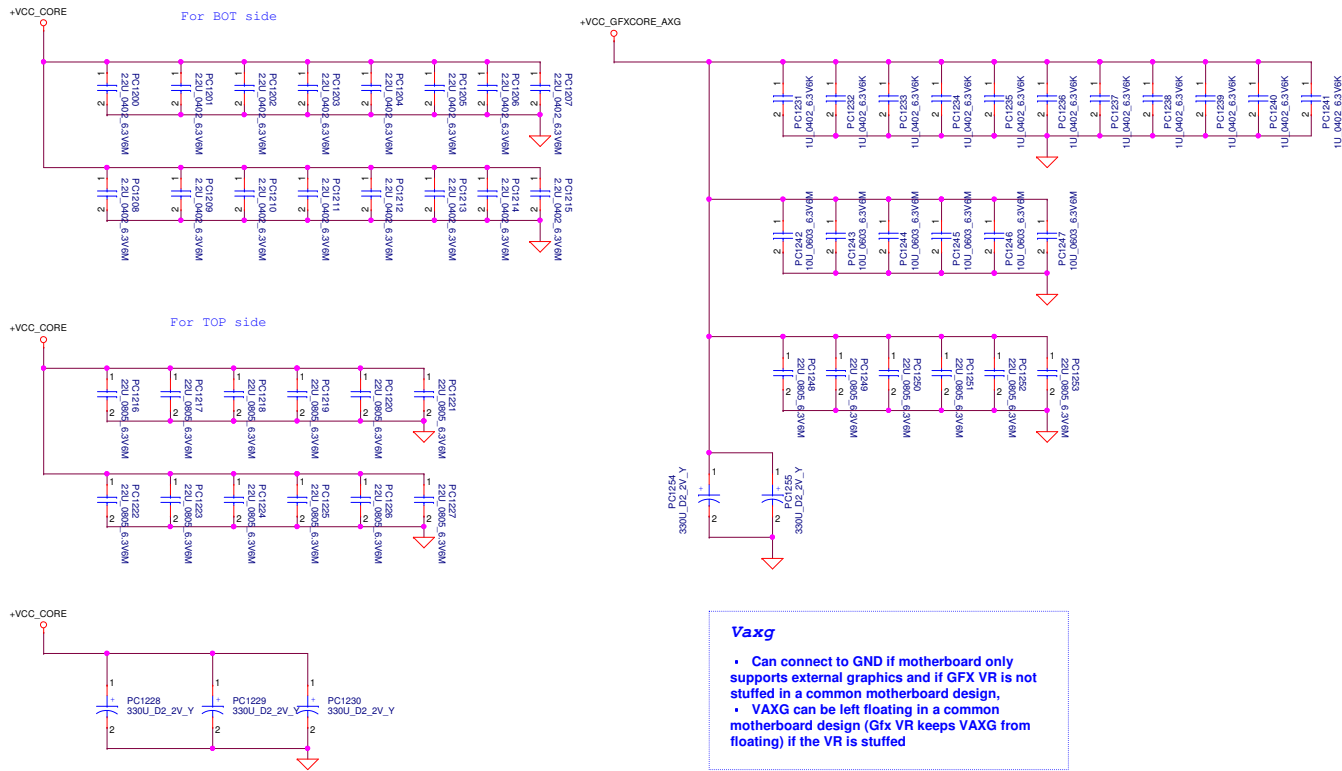
| GPU_VID5<br>(GPIO_10) | GPU_VID4<br>(GPIO_14) | GPU_VID3<br>(GPIO_15) | GPU_VID2<br>(GPIO_16) | GPU_VID1<br>(GPIO_20) | Core Voltage Level |
|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|--------------------|
| 1                     | 0                     | 0                     | 1                     | 0                     | 1.05V              |
| 1                     | 0                     | 1                     | 0                     | 0                     | 1V                 |
| 1                     | 0                     | 1                     | 1                     | 0                     | 0.95V              |
| 1                     | 1                     | 0                     | 0                     | 0                     | 0.9V               |

**+VGA\_CORE**  
TDC 20A  
Peak Current 30A  
OCP current 36A  
FSW=350kHz  
DCR 1.1mohm +/-5%

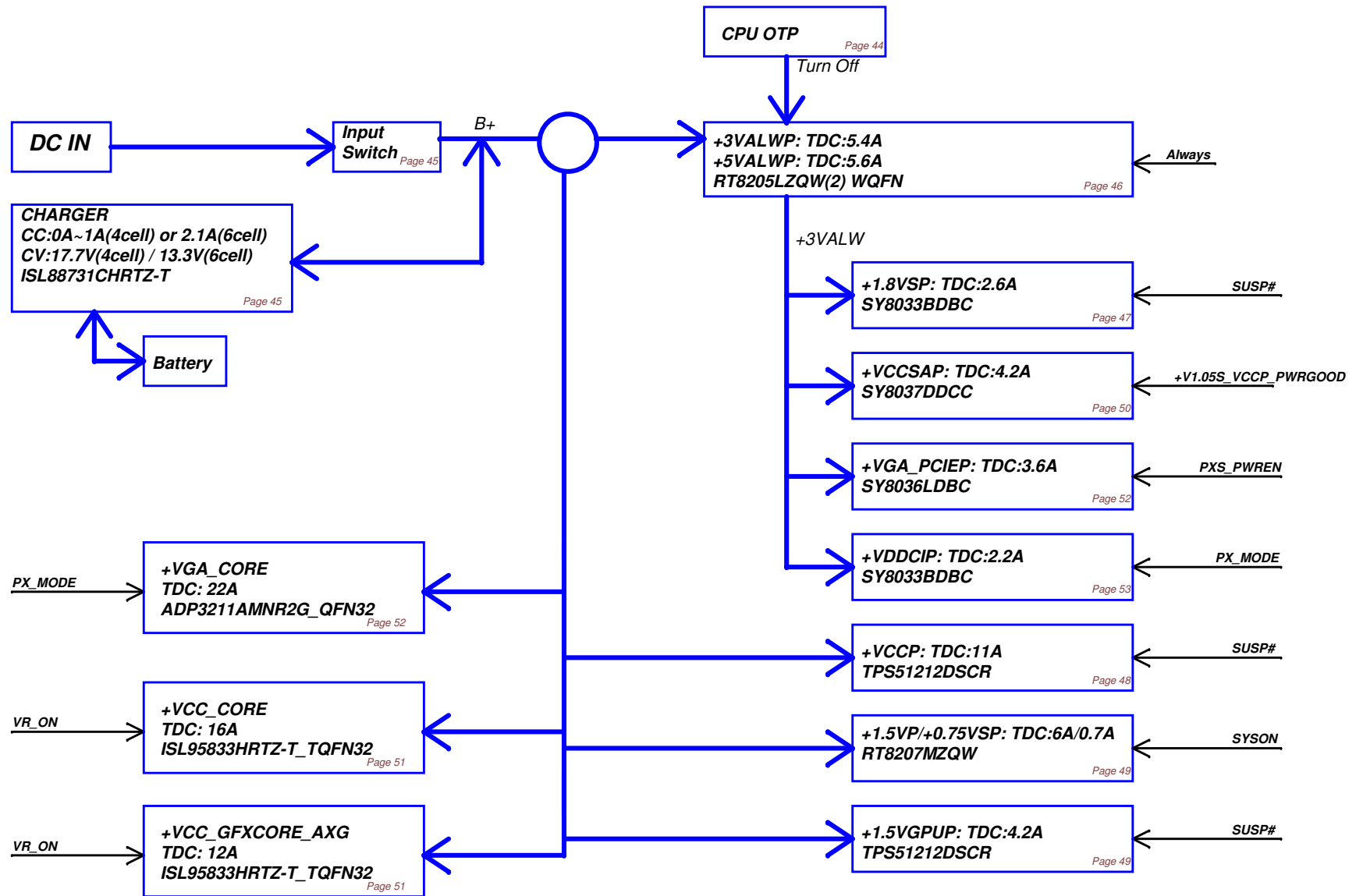


|          | Thames XT | Mars Pro |
|----------|-----------|----------|
| VGA_PCIE | 1.0V      | 0.95V    |
| PR832    | 6.81K     | 5.9K     |





# Power block



## Page 1

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|   |                    |                 |            |  |                           |                |
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